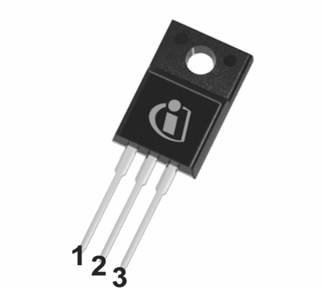
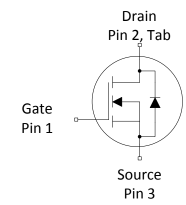
MOSFET

650V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

PG-TO 220 FP





Features

- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- JEDEC qualfied, Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor Lighting

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$R_{DS(on),max}$	400	mΩ
$I_{D.}$	15.1	A
$Q_{g.typ}$	39	nC
$I_{D,pulse}$	30	A
E_{oss}@400V	2.8	µJ

Type / Ordering Code	Package	Marking	Related Links
IPA65R400CE	PG-TO 220 FullPAK	65S400CE	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	15.1 9.5	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	30	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	215	mJ	I_D=1.8A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.32	mJ	I_D=1.8A; V_{DD}=50V; see table 10
Avalanche current, repetitive	I_{AR}	-	-	1.8	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS}=0...480V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation (Non FullPAK) TO-252, TO-251	P_{tot}	-	-	118	W	T_C=25°C
Power dissipation (FullPAK) TO-220FP	P_{tot}	-	-	31	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Continuous diode forward current	I_S	-	-	10.6	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	30	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 8
Maximum diode commutation speed	di_f/dt	-	-	500	A/µs	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 8
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$. TO251 equivalent, Maximum duty cycle D=0.5
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics (FullPAK) TO-220FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	V_{DS}=V_{GS}, I_D=0.32mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=650, V_{GS}=0V, T_j=25°C V_{DS}=650, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.36 0.94	0.40 -	Ω	V_{GS}=10V, I_D=3.2435A, T_j=25°C V_{GS}=10V, I_D=3.2435A, T_j=150°C
Gate resistance	R_G	-	17	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	710	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Output capacitance	C_{oss}	-	41	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	32	-	pF	V_{GS}=0V, V_{DS}=0...480V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	140	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...480V
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.86525A, R_G=4.9Ω; see table 9
Rise time	t_r	-	12	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.86525A, R_G=4.9Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	110	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.86525A, R_G=4.9Ω; see table 9
Fall time	t_f	-	11	-	ns	V_{DD}=400V, V_{GS}=13 V, I_D=4.86525A, R_G=4.9Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	4	-	nC	V_{DD}=480V, I_D=4.86525A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	20	-	nC	V_{DD}=480V, I_D=4.86525A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	39	-	nC	V_{DD}=480V, I_D=4.86525A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	V_{DD}=480V, I_D=4.86525A, V_{GS}=0 to 10V

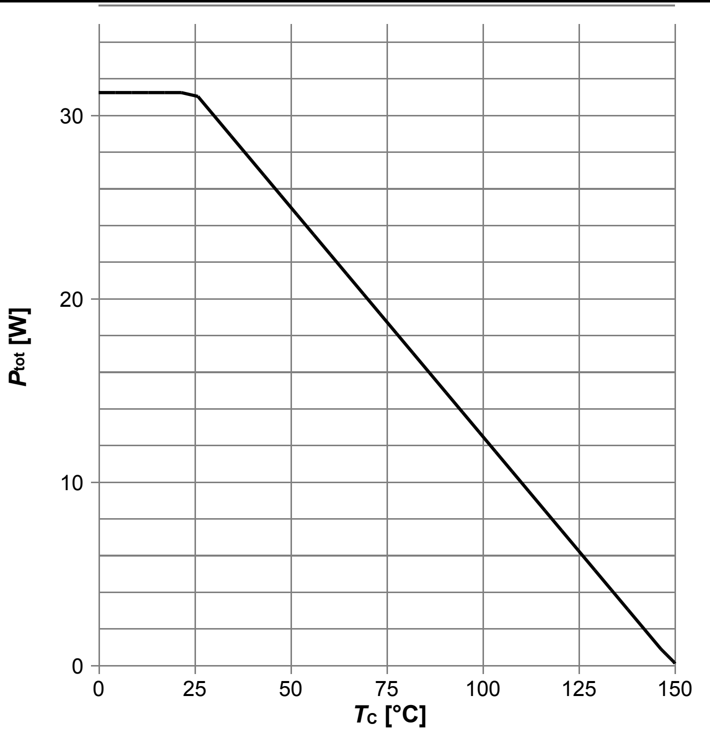
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 480V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 480V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=4.9A, T_j=25°C
Reverse recovery time	t_{rr}	-	280	-	ns	V_R=400V, I_F=4.9A, di_F/dt=100A/µs; see table 19
Reverse recovery charge	Q_{rr}	-	2.8	-	µC	V_R=400V, I_F=4.9A, di_F/dt=100A/µs; see table 19
Peak reverse recovery current	I_{rrm}	-	17	-	A	V_R=400V, I_F=4.9A, di_F/dt=100A/µs; see table 19

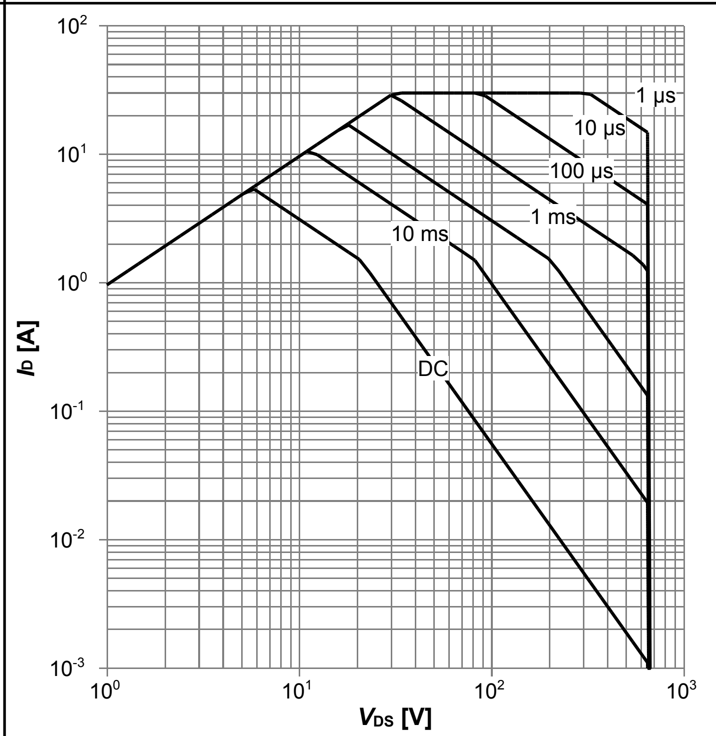
4 Electrical characteristics diagrams

Diagram 1: Power dissipation (FullPAK)



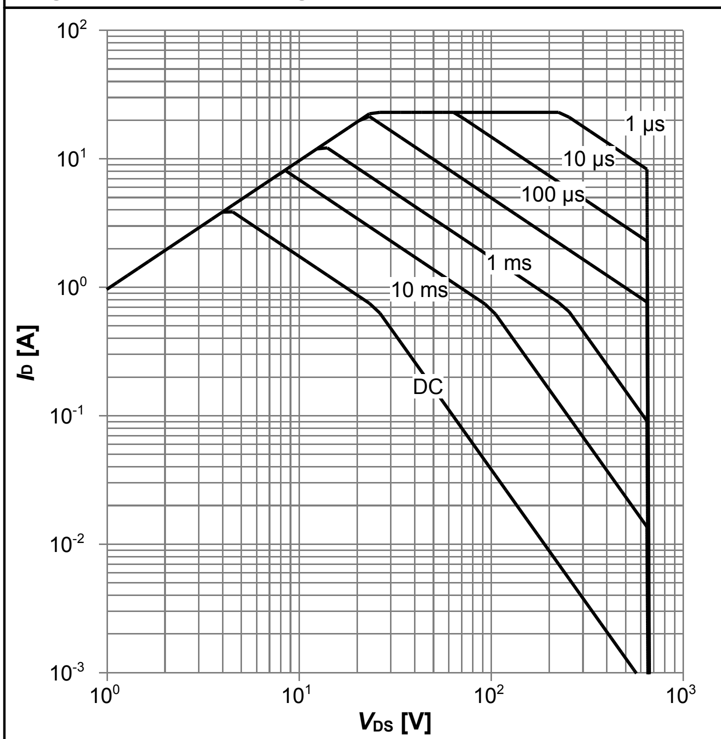
P_{tot}=f(T_C)

Diagram 2: Safe operating area (FullPAK)



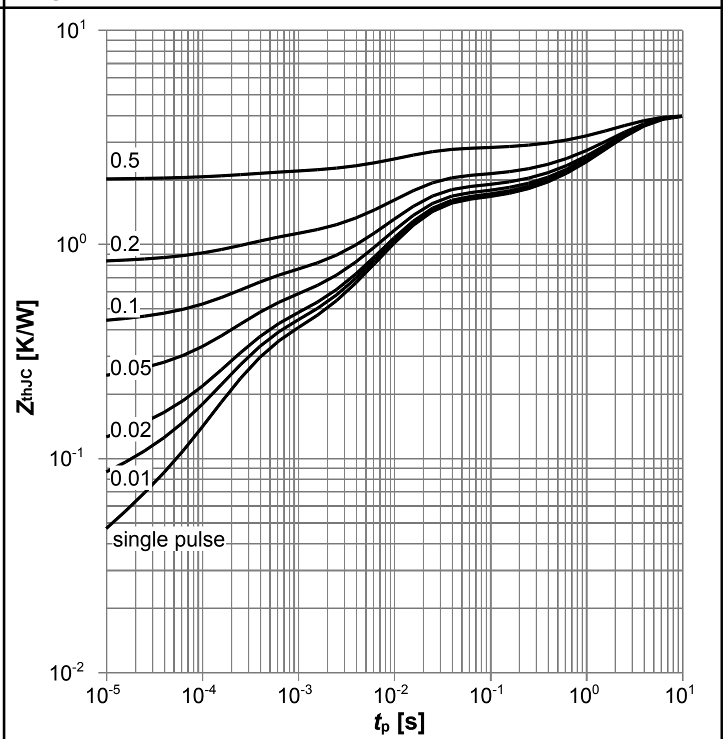
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area (FullPAK)



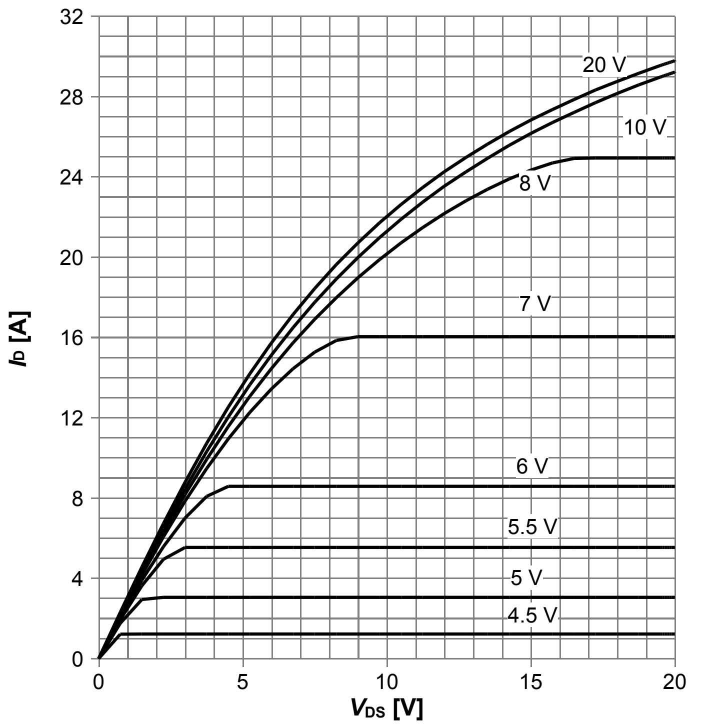
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance (FullPAK)



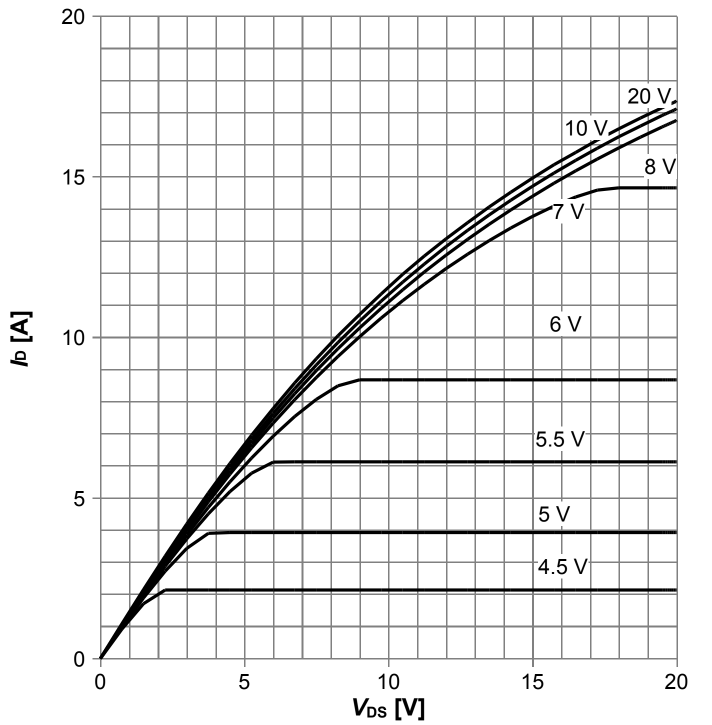
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



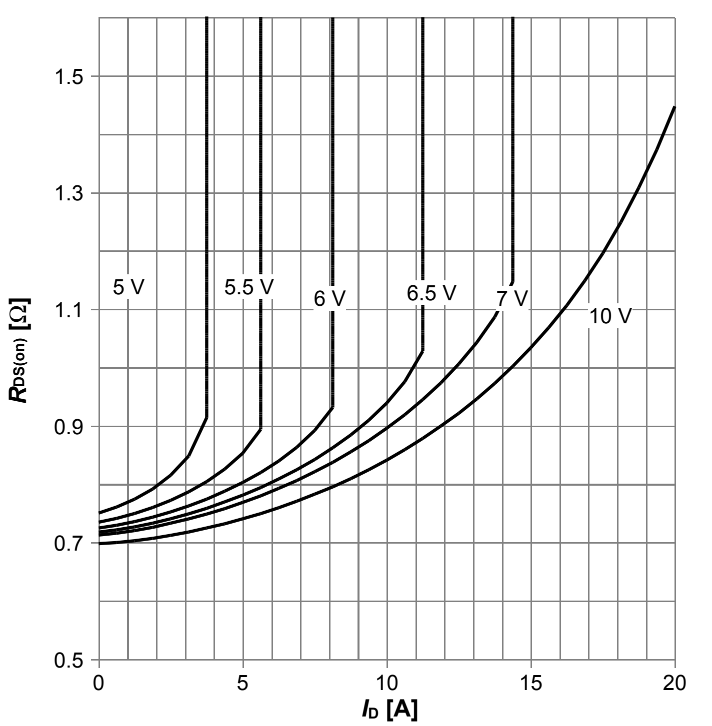
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



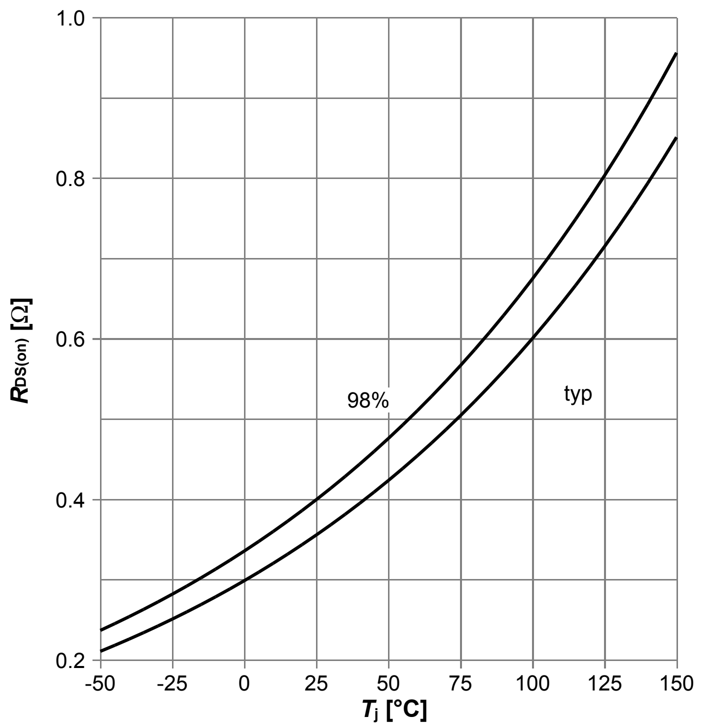
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



$R_{DS(on)}$=f(T_j); I_D=3.2A; V_{GS}=10 V

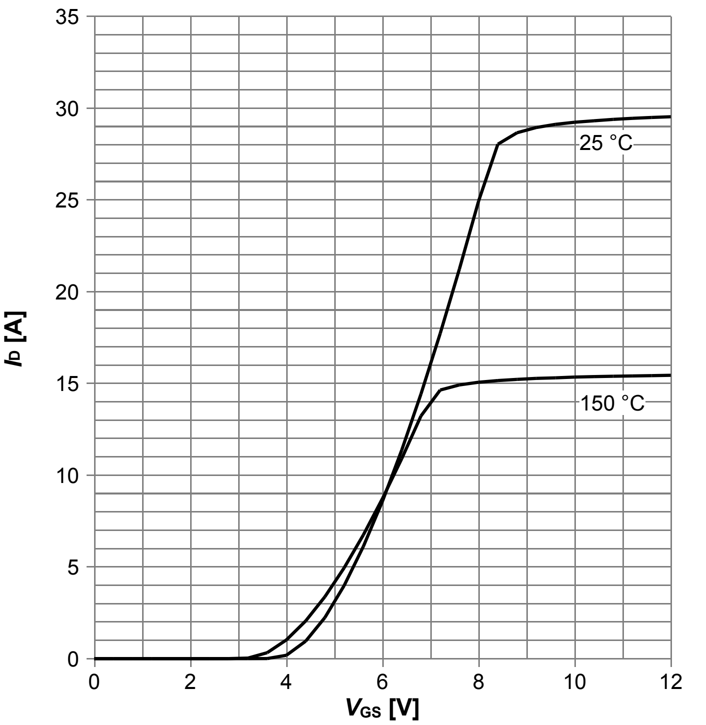
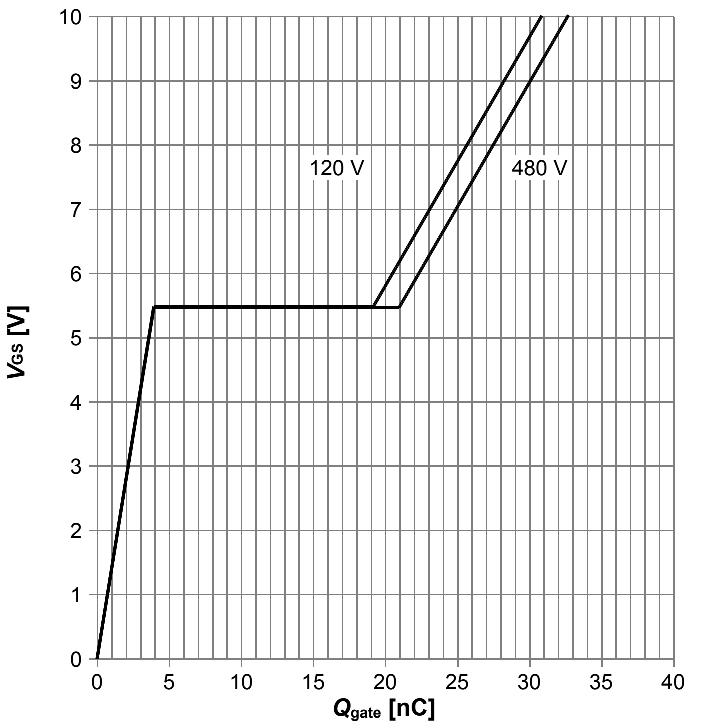
Diagram 9: Typ. transfer characteristics	Diagram 10: Typ. gate charge
	
$I_D=f(V_{GS})$; V_{DS}=20V; parameter: T_j	$V_{GS}=f(Q_{gate})$; I_D=4.9 A pulsed; parameter: V_{DD}

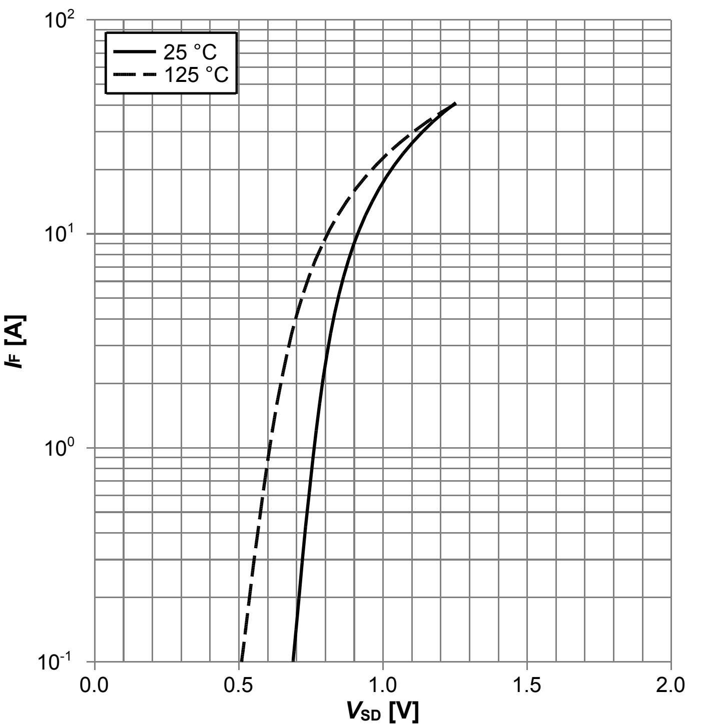
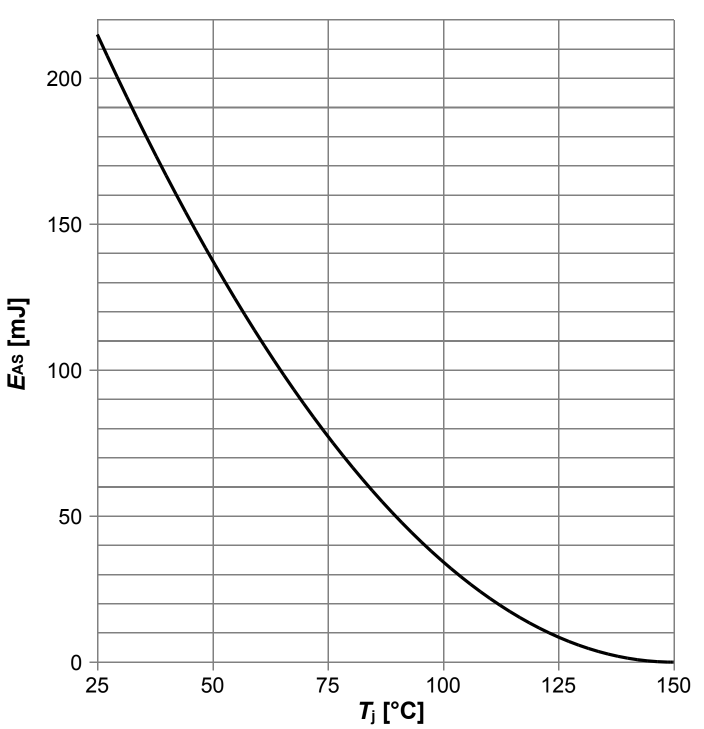
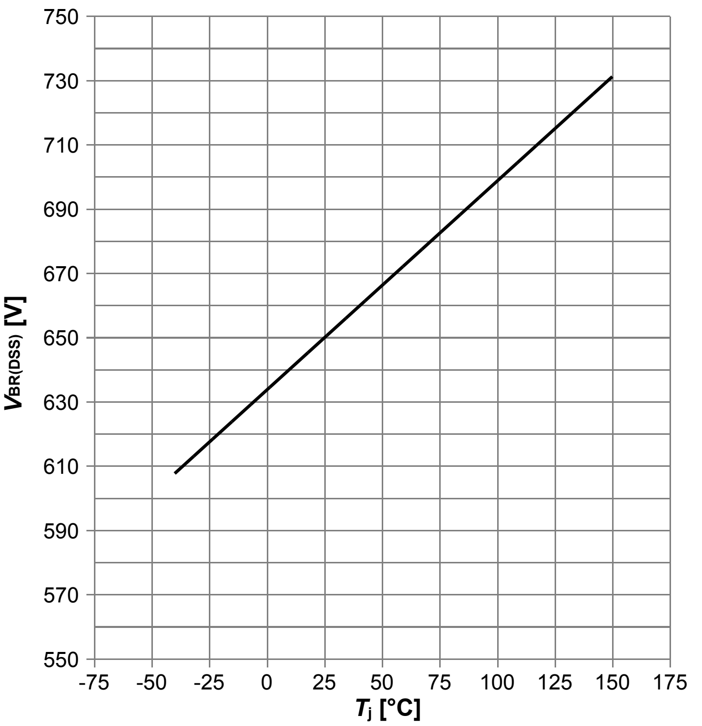
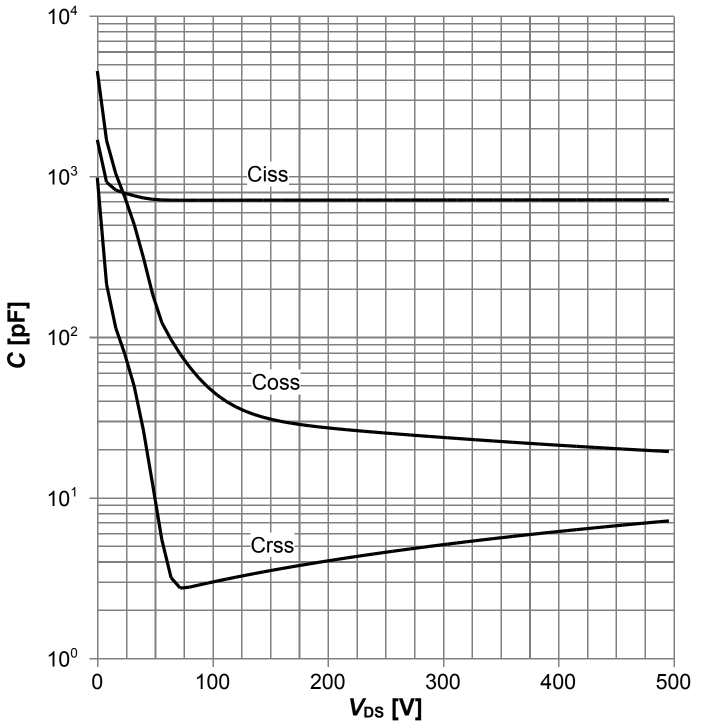
Diagram 11: Forward characteristics of reverse diode	Diagram 12: Avalanche energy
	
$I_F=f(V_{SD})$; parameter: T_j	$E_{AS}=f(T_j)$; I_D=1.8 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



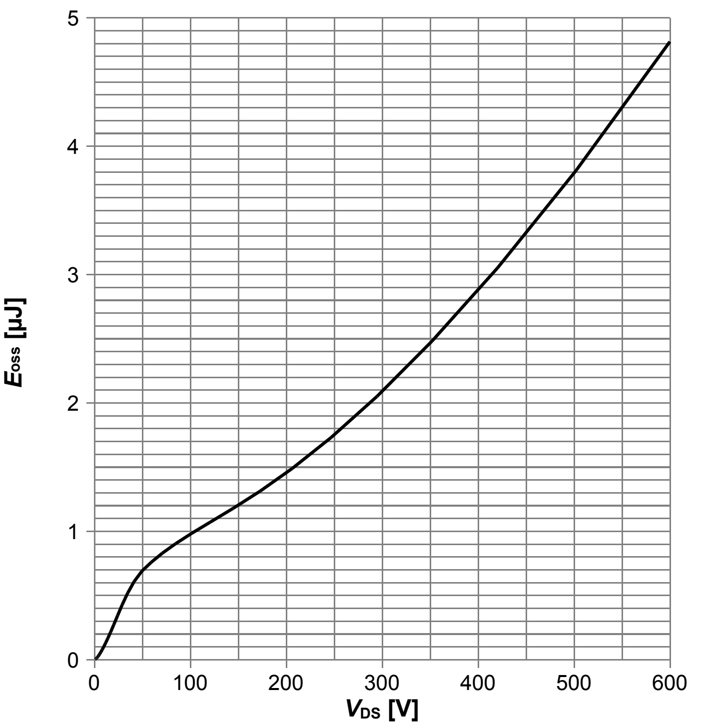
$V_{BR(DSS)}$=f(T_j); I_D=1.0 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

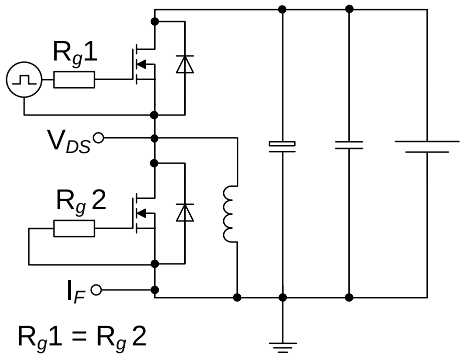
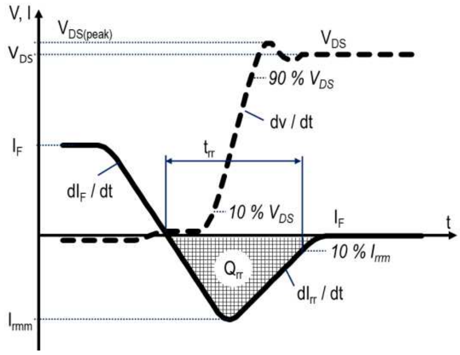
<table>
<tr><th>Test circuit for diode characteristics</th><th>Diode recovery waveform</th></tr>
<tr><td>
</td><td>
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Table 9 Switching times

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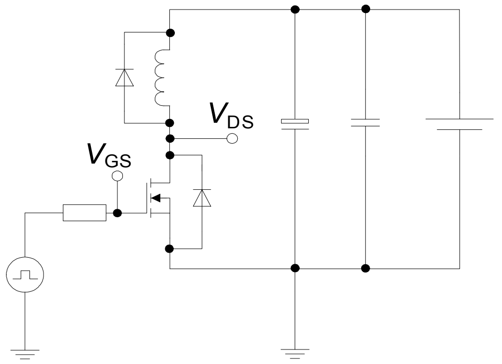
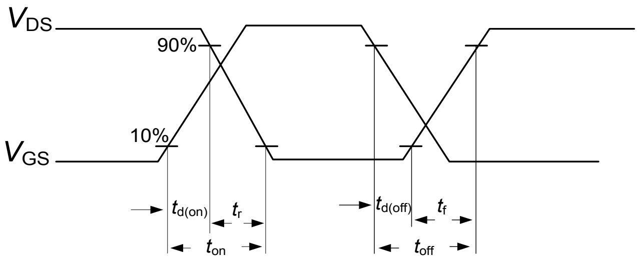
<tr><th>Switching times test circuit for inductive load</th><th>Switching times waveform</th></tr>
<tr><td>
</td><td>
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Table 10 Unclamped inductive load

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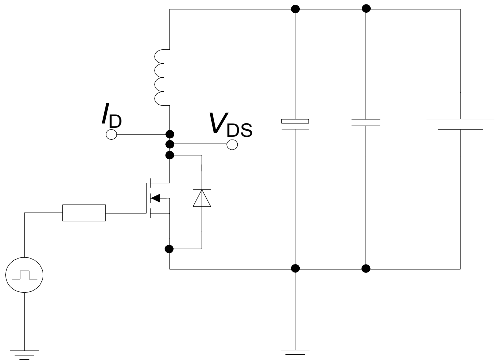
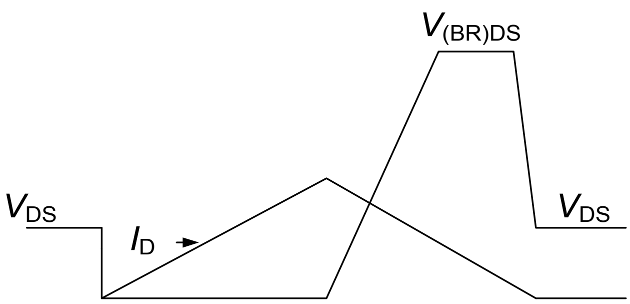
<tr><th>Unclamped inductive load test circuit</th><th>Unclamped inductive waveform</th></tr>
<tr><td>
</td><td>
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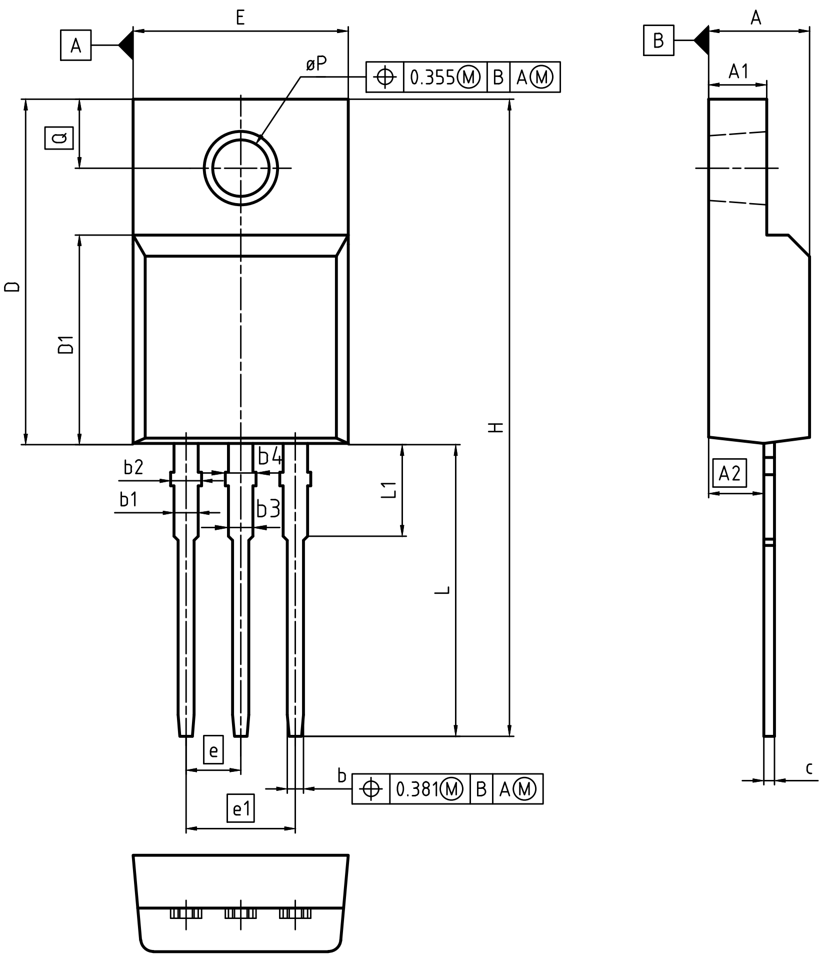
6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

Dimensions do not include mold flash, protrusions or gate burrs

DOCUMENT NO.
Z8B00003319

SCALE 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
05-05-2014

REVISION
04

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ CE Webpage: www.infineon.com
- IFX CoolMOS™ CE application note: www.infineon.com
- IFX CoolMOS™ CE simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPA65R400CE

Revision: 2017-04-19, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-02-24	Release of final version
2.1	2017-04-19	Modified Rg value in Table 6 and timing value in Table 7

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Published by
Infineon Technologies AG
81726 München, Germany

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