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UCC28811DR

TI,Texas Instruments

LED Lighting Drivers LED Lighting Power Controller

LED LIGHTING POWER CONTROLLER

FEATURES

- **Transition Mode Controller for Low Implementation Cost of AC Input LED Lighting Applications**
- **Implements Single Stage Power Factor Corrected LED Driver**
- **Enhanced Transient Response With Slew-Rate Comparator**
- **Interfaces with Traditional Wall Dimmers**
- **Accurate Internal V_{REF} for Tight Output Regulation**
- **Two UVLO Options**
- **Overvoltage Protection (OVP), Open-Feedback Protection and Enable Circuits**
- **±750-mA Peak Gate Drive Current**
- **Low Start-Up and Operating Currents**
- **Lead (Pb)-Free Packages**

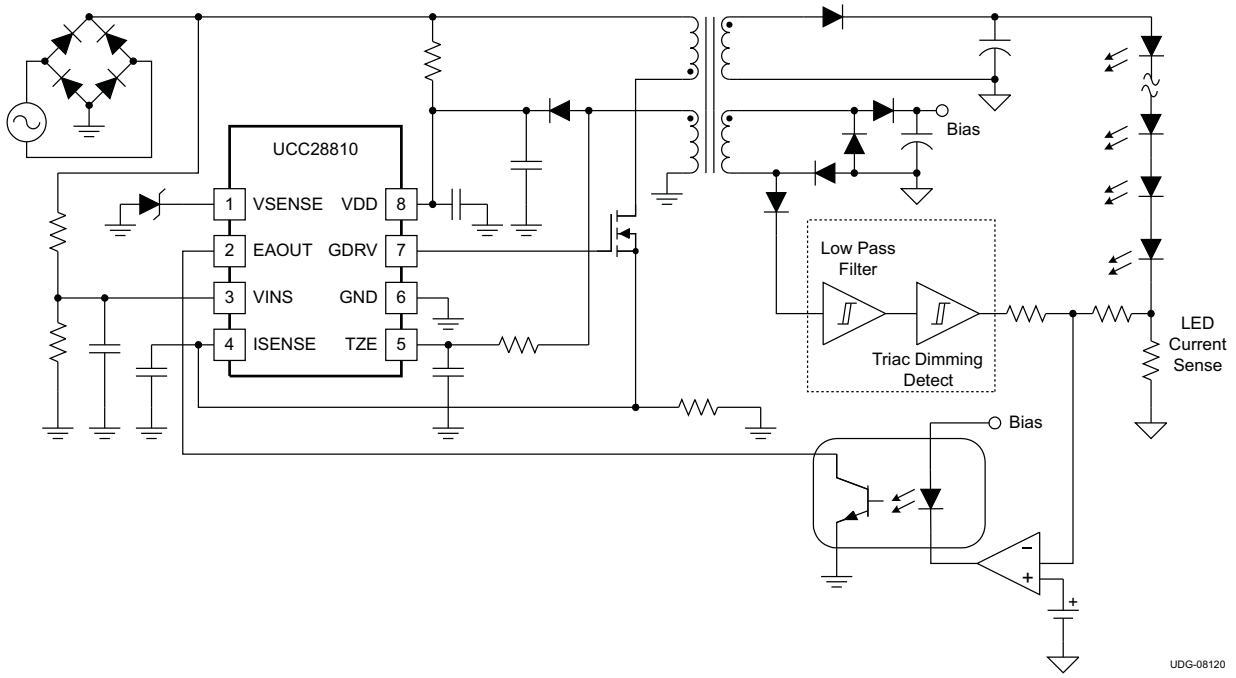
APPLICATIONS

- **AC Input General Lighting Applications Using HB LEDs**
- **Industrial, Commercial and Residential Lighting Fixtures**
- **Outdoor Lighting: Street, Roadway, Parking, Construction and Ornamental LED Lighting Fixtures**

DESCRIPTION

The UCC28810 and UCC28811 are general lighting power controllers for low to medium power lumens applications requiring power factor correction and EMC compliance. It is designed for controlling a flyback, buck or boost converter operating in critical conduction mode. It features a transconductance voltage amplifier for feedback error processing, a simple current reference generator for generating a current command proportional to the input voltage, a current-sense (PWM) comparator, PWM logic and a totem-pole driver for driving an external FET.

SIMPLIFIED APPLICATION DIAGRAM



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DESCRIPTION (CONTINUED)

In the critical conduction mode operation, the PWM circuit is self-oscillating with the turn-on being governed by a transformer zero energy detector (TZE pin) and the turn-off being governed by the current sense comparator. Additionally, the controller provides features such as peak current limit, restart timer, overvoltage protection (OVP), and enable.

The efficient system performance is attained by incorporation of zero power detect function which allows the controller output to shut down at light load conditions without running into overvoltage. The device also features an innovative slew rate enhancement circuit which improves the large signal transient performance of the voltage error amplifier. The low start-up and operating currents of the device result in low power consumption and ease of start-up. The highly-accurate internal bandgap reference leads to tight regulation of the output voltage in normal and OVP conditions, resulting in higher system reliability. The enable comparator ensures that the controller is off if the feedback sense path is broken or if the input voltage is very low.

There are two key parametric differences between UCC28810 and UCC28811, the UVLO turn-on threshold and the g_M amplifier source current. The UVLO turn-on threshold of the UCC28810 is 15.8 V and for the UCC28811 it is 12.5 V. The g_M amplifier source current for UCC28810 is typically 1.3 mA, and for the UCC28811 it is 300μA. The higher UVLO turn-on threshold of the UCC28810 allows quicker and easier start-up with a smaller VDD capacitance while the lower UVLO turn-on threshold of UCC28811 allows operation of the critical conduction mode controller to be easily controlled by the downstream PWM controller in two-stage power converters. The UCC28810 g_M amplifier also provides a full 1.3-mA typical source current for faster start-up and improved transient response when the output is low either at start-up or during transient conditions. The UCC28811 is suitable for applications such as street lights and larger area luminaires where a two-stage power conversion is needed. The UCC28810 is suitable for applications such as commercial or residential retrofit luminaires where there is no down-stream PWM conversion and the advantages of smaller VDD capacitor and improved transient response can be realized.

Devices are available in the industrial temperature range of –40°C to 105°C. Package offering is an 8-pin SOIC (D) package.

ORDERING INFORMATION(1)

$T_A = T_J$	UVLO THRESHOLD VOLTAGE (V)		g_M AMPLIFIER SOURCE CURRENT (μA)	PACKAGE	PIN COUNT	SUPPLY	ORDERABLE DEVICE NUMBER
	ON	OFF					
–40°C to 105°C	15.8	9.7	–1300	D	8	Tube of 80	UCC28810D
						Reel of 2500	UCC28810DR
	12.5	9.7	–300			Tube of 80	UCC28811D
						Reel of 2500	UCC28811DR

(1) D (SOIC-8) package is available taped and reeled. Add R suffix to device type (e.g. UCC28810DR) to order quantities of 2,500 devices per reel.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Input voltage	VDD (Internally clamped)	20	V
	VSENSE, VINS, ISENSE	5	
Minimum input voltage	VSENSE, VINS, ISENSE	–5	
Input current	VDD	30	mA
	TZE	±10	
Output current	GDRV	±750	mA
Output voltage	GDRV	–5	V
T_{stg} Storage temperature		–55 to 150	°C
T_J Operating temperature		–65 to 150	
Soldering temperature		300	

(1) Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability. Currents are positive into, and negative out of the specified terminal.

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT (°C/W)
Plastic 8-Pin Small Outline	150

(1) TI device packages are modeled and tested for thermal performance using printed circuit board designs outlined in JEDEC standards JESD 51-3 and JESD 51-7.

ELECTRICAL CHARACTERISTICS

–40°C ≤ T_A = T_J ≤ 105°C, V_{VDD} = 12 V_{DC}, C_{GDRV} = 0.1-µF from VDD to GND, all voltages are with respect to GND.

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
V_{VDD}	Operating voltage					18	V
	Shunt voltage		I_{VDD} = 25 mA	18	19	20	
	Supply current, off		V_{VDD} = V_{VDD} turn-on threshold –300 mV		75	125	µA
	Supply current, disabled		V_{VSENSE} = 0.5 V		2	4	mA
I_{VDD}	Supply current, on		75 kHz, C_{GDRV} = 0 nF		4	6	
	Supply current, dynamic operating		75 kHz, C_{GDRV} = 1 nF		5	7	
UVLO							
	VDD turn-on threshold	UCC28810		15.4	15.8	16.4	V
		UCC28811		12.0	12.5	13.0	
	VDD turn-off threshold			9.4	9.7	10.0	
V_{UVLO}	UVLO hysteresis	UCC28810		5.8	6.3	6.8	V
		UCC28811		2.3	2.8	3.3	
VOLTAGE AMPLIFIER (VSENSE)							
V_{REF}	Internal voltage reference			2.45	2.50	2.55	V
I_{BIAS}	Input bias current					0.5	µA
	EAOUT high		V_{VSENSE} = 2.1 V	4.5		5.5	V
	EAOUT low		V_{VSENSE} = 2.55 V		1.80	2.45	V
g_M	Transconductance		T_J = 25°C, V_{EAOUT} = 3.5 V	60	90	130	µS
$I_{EAOUT,SRC}$	Source current	UCC28810	V_{VSENSE} = 2.1 V, V_{EAOUT} = 3.5 V	–0.2	–1.0		mA
		UCC28811		–200	–300	–400	µA
$I_{EAOUT,SNK}$	Sink current		V_{VSENSE} = 2.1 V, V_{EAOUT} = 3.5 V	0.2	1.0		mA
OVERVOLTAGE PROTECTION / ENABLE (VSENSE)							
$V_{OV(ref)}$	Overvoltage reference	UCC28810		V_{VREF}+ 0.165	V_{VREF} +0.190	V_{VREF} +0.210	V
		UCC28811		V_{VREF}+ 0.150	V_{VREF}+ 0.180	V_{VREF}+ 0.210	
	Hysteresis	UCC28810		175	200	225	mV
		UCC28811		150	180	210	
	Enable threshold	UCC28810		0.62	0.67	0.72	V
		UCC28811		0.18	0.23	0.28	
	Enable hysteresis			0.05	0.10	0.20	V
CURRENT REFERENCE GENERATOR							
K	Current reference generator gain constant		V_{VINS} = 0.5 V, V_{EAOUT} = 3.5 V	0.43	0.65	0.87	1/V
	Dynamic input range, V_{VINS} INPUT			0 to 2.5	0 to 3.5		V
V_{EAOUT}	Error amplifier dynamic input range			2.5 to 3.8	2.5 to 4.0		V
	Input bias current, VINS				0.1	1.0	µA

ELECTRICAL CHARACTERISTICS (continued)

–40°C ≤ T_A = T_J ≤ 105°C, V_{VDD} = 12 V_{DC}, C_{GDRV} = 0.1-µF from VDD to GND, all voltages are with respect to GND.

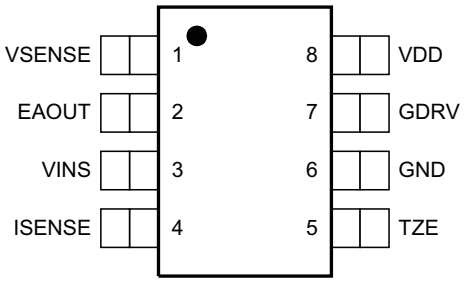
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ZERO POWER						
V_{EAOUT}	Zero power comparator threshold(1)		2.1	2.3	2.5	V
TRANSFORMER ZERO ENERGY DETECT						
	Input threshold (rising edge)(1)		1.00	1.25	1.80	V
	Hysteresis(1)		250	350	450	mV
	Input high clamp	I_{TZE} = 3 mA		5	6	V
	Input low clamp	I_{TZE} = –3 mA	0.30	0.65	0.90	V
t_{RSRT}	Restart time delay		200	400		µs
CURRENT SENSE COMPARATOR						
I_{BIAS}	Input bias current	V_{ISENSE} = 0 V		0.1	1.0	µA
	Input offset voltage(1)		–10		10	mV
t_{DLY}	Delay to output	ISENSE to GDRV		300	400	ns
	Maximum current sense threshold voltage		1.55	1.70	1.80	V
PFC GATE DRIVER						
R_{PULLUP}	GDRV pull up resistance	I_{GDRV} = –125 mA		5	12	Ω
R_{PULLDN}	GDRV pull down resistance	I_{GDRV} = 125 mA		2	10	Ω
t_{RISE}	GDRV output rise time	C_{GDRV} = 1 nF, R_{GRDV} = 10 Ω		25	75	ns
t_{FALL}	GDRV output fall time	C_{GDRV} = 1 nF, R_{GRDV} = 10 Ω		10	50	ns

(1) Ensured by design. Not production tested.

Table 1. PIN DESCRIPTIONS

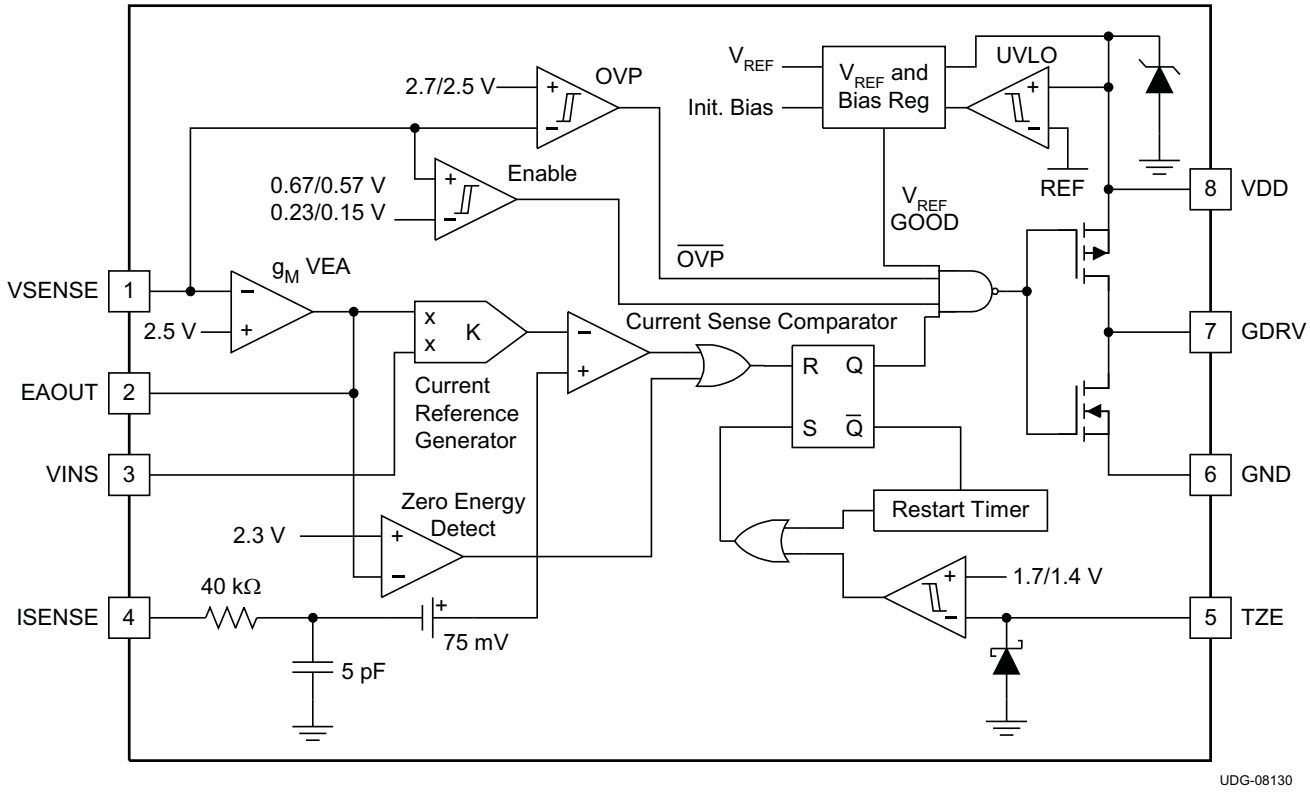
TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EAOUT	2	O	Output of the transconductance error amplifier. The output current capability of this pin is 10 μA under normal conditions, but increases to 1 mA when the voltage on VSENSE rises above 2.5 V. The EAOUT voltage is one of the inputs to the current reference generator, with a dynamic input range of 2.5 V to 4.0 V. During zero energy or overvoltage conditions, this pin goes below 2.5 V, nominal. When it goes below 2.3 V, the zero energy detect comparator is activated which prevents the gate drive from switching. Loop compensation components are connected between this pin and ground, or can be connected directly to the collector of the opto coupler in isolated applications.
GND	6	–	The device reference ground. All bypassing elements are connected to the GND pin with the shortest traces possible.
GDRV	7	O	The gate drive output driving the flyback, buck, or boost switch. This output is capable of delivering up to 750-mA peak currents during turn-on and turn-off. An external gate drive resistor may be needed to limit the peak current depending upon the VDD voltage being used. Below the UVLO threshold, the output is held low.
ISENSE	4	I	This pin senses the instantaneous switch current in the external switch and uses this signal as the internal ramp for the current sense comparator. A small internal noise filter is provided. If additional filtering is needed, an external R-C filter may be added to further suppress noise spikes. An internal clamp on the current reference generator output terminates the switching cycle if V_{ISENSE} exceeds 1.7 V. An internal 75-mV offset is added to ISENSE signal to limit the zero crossing distortion. The ISENSE threshold voltage is approximately equal to: $V_{ISENSE} \cong 0.67 \times (V_{EAOUT} - 2.5\,V) \times (V_{VINS} + 75\,mV)$
TZE	5	I	This pin is the input for the transformer zero energy detect comparator. A bias winding can be used to sense the transformer zero energy. The transition is detected when the inductor current falls to zero and the TZE input goes low. Internal active clamps are provided to prevent TZE from going below ground or rising too high. If zero energy is not detected within 400 μs, a restart timer sets the latch and the gate drive high.
VDD	8	I	The supply voltage for the device. This pin must be bypassed with a high-frequency capacitor (not less than 0.1 μF) and tied directly to GND with the shortest traces possible. The UCC28810 has a wide UVLO hysteresis, typically 6.3 V, which allows use of a lower value holdup capacitor on VDD, resulting in faster start up. The UCC28811 has a narrow UVLO hysteresis, typically 2.8 V, and a typical turn-on threshold of 12.5 V for applications where the device needs to be controlled by a downstream PWM controller. This narrower UVLO hysteresis requires a larger value holdup capacitor.
VINS	3	I	This pin senses the instantaneous regulator input voltage through an external voltage divider. The VINS voltage acts as one of the inputs to the current reference generator. The recommended operating range is 0 V to 3.8 V at high line.
VSENSE	1	I	This pin is the inverting input to the transconductance amplifier, with a nominal value of 2.5 V, and is also the input to the OVP comparator. Pulling this pin below the ENABLE threshold turns off the output switching, providing the ability to externally disable the converter. This function also provides feedback fault protection, ensuring no runaway if the feedback path is open. When using the internal error amplifier, this pin senses the output voltage through a voltage divider.

SOIC-8 PACKAGE (TOP VIEW)



BLOCK DESCRIPTION

BLOCK DIAGRAM



UVLO and Reference Circuit

This circuitry generates a precision reference voltage used to obtain a tightly controlled UVLO threshold. In addition to generating a 2.5-V reference for the noninverting terminal of the g_M amplifier, it generates the reference voltages for OVP, enable, zero energy detect and the current reference generator circuits. An internal rail of 7.5 V is also generated to drive all the internal circuitry.

Error Amplifier

The voltage error amplifier in the UCC2881x is a transconductance amplifier with a typical transconductance value of 90 µS. The advantage in using a transconductance amplifier is that the inverting input of the amplifier is solely determined by the external resistive-divider from the output voltage and not the transient behavior of the amplifier itself. This allows the VSENSE pin to be used for sensing over voltage conditions.

The sink and source capability of the error amplifier is approximately 10 µA during normal operation of the amplifier. But when the VSENSE pin voltage is beyond the normal operating conditions (V_{VSENSE} >1.05 × V_{REF}, V_{VSENSE} < 0.88 × V_{REF}), additional circuitry to enhance the slew-rate of the amplifier is activated. Enhanced slew-rate of the compensation capacitor results in a faster start-up and transient response. This prevents the output voltage from drifting too high or too low, which can happen if the compensation capacitor were to be driven by the normal drive current of 10-µA. When VSENSE rises above the normal range, the enhanced sink current capability increases to 1 mA, nominal. When VSENSE falls below the normal range, the UCC28810 can source more than 1 mA and the UCC28811 sources approximately 300 µA. The limited source current in the UCC28811 helps to gradually increase the error voltage on the EAOUT pin preventing a step increase in line current. The actual rate of increase of the voltage on the EAOUT pin is dependent on the compensation network externally connected to the EAOUT pin.

Transformer Zero Energy Sense and Restart Timer Circuits

When all of the energy stored in the transformer has been delivered to the load, the voltage across the primary winding falls to zero. This voltage can be sensed by monitoring the bias winding of the transformer. The internal active clamp circuitry prevents the voltage from going to a negative or a high positive value. The clamp has the capability to sink and source 10 mA. The resistor value in series with the bias winding should be chosen to limit the pin current to less than 10 mA under all operating conditions. The rising edge threshold of the TZE sense comparator can be as high as 2.0 V. If the bias winding is not used to power the controller then it should be chosen such that the positive voltage (when the power MOSFET is off) at the TZE pin is greater than 2.0 V, limited to less than 10 mA.

The restart timer attempts to set the gate drive high when the gate drive remains off for more than 400 µs nominally. The minimum time period of the timer is 200 µs. This translates to a minimum switching frequency of 5 kHz. The primary inductance value is chosen for switching frequencies greater than 5 kHz.

Enable Circuit

The gate drive signal is held low if the voltage at the VSENSE pin is less than the ENABLE threshold. This feature can be used to disable the converter by pulling VSENSE low. If the output feedback path is broken, VSENSE is pulled to ground and the output is disabled to protect the power stage.

Zero Energy Detect Circuit

When the output of the g_M amplifier goes below 2.3 V, the zero power comparator latches the gate drive signal low. The slew rate enhancement circuitry of the g_M amplifier that is activated during overvoltage conditions slews the EAOUT pin to approximately 2.4 V. This ensures that the zero power comparator is not activated during transient behavior (when the slew rate enhancement circuitry is activated).

Current Reference Generator Circuit

The current reference generator has two inputs. One is the error amplifier output voltage (V_{EAOUT}), while the other is instantaneous input voltage sense (V_{VINS}) which is obtained by a resistive divider from the rectified line. The current reference generator creates a current sense threshold signal that is approximately equal to 0.67 × V_{VINS} × (V_{EAOUT}–2.5 V). There is a positive offset of 75 mV added to the VINS signal in order to improve the zero-crossing distortion and hence the THD performance of the controller in the application. The dynamic range of the inputs can be found in the electrical characteristics table.

Overvoltage Protection (OVP) Circuit

The OVP feature in this device is not activated under most operating conditions because of the presence of the slew rate enhancement circuitry present in the error amplifier. As soon as the output voltage reaches 5% to 7% above the nominal value, as detected by VSENSE, the slew rate enhancement circuit is activated, and the error amplifier output voltage is pulled below the dynamic range of the current reference generator. This prevents further rise in the output voltage.

If the EAOUT pin is not pulled low fast enough, and the output voltage rises further, the OVP circuit acts as a second line of protection. When the voltage at the VSENSE pin is more than 7.5% of the nominal value [>(V_{REF}+0.190)], the OVP feature is activated. It stops the gate drive from switching as long as the voltage at the VSENSE pin is above the nominal value (V_{REF}). This prevents the output dc voltage from going above 7.5% of the regulated value, and protects the other components of the system.

TYPICAL CHARACTERISTICS

Unless otherwise noted, V_{VDD}=12 V, –40°C ≤ T_A = T_J ≤ 105°C

GDRV SATURATION VOLTAGE vs GDRV SOURCE CURRENT

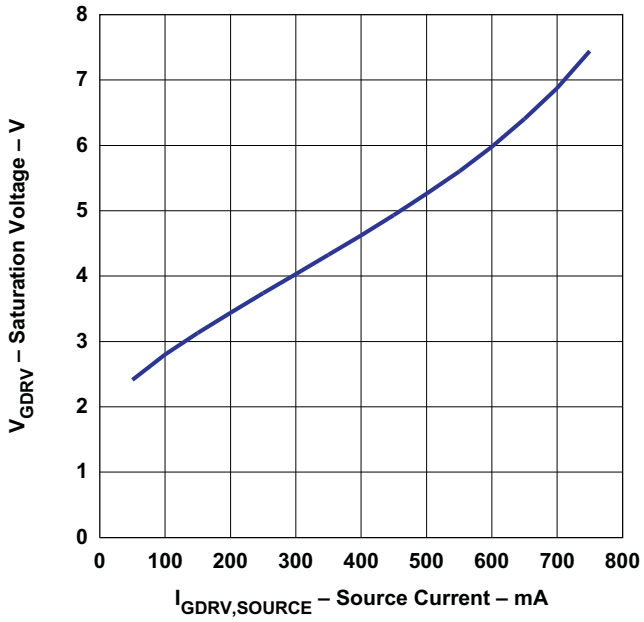


Figure 1.

GDRV SATURATION VOLTAGE vs GDRV SINK CURRENT

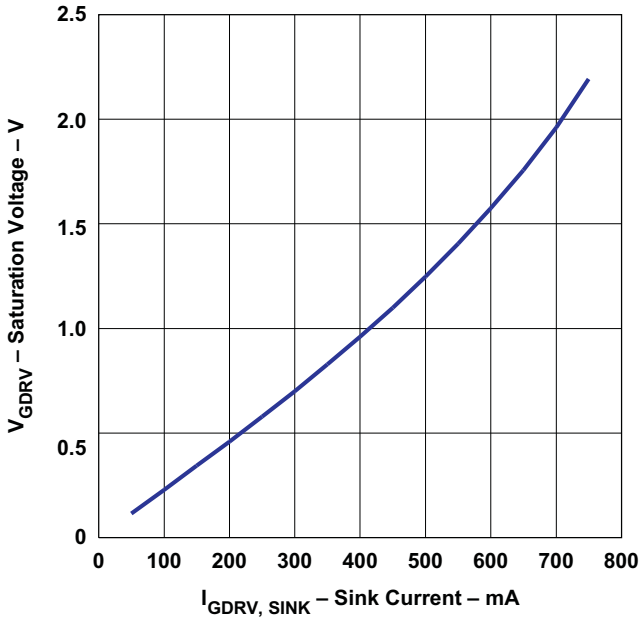


Figure 2.

SUPPLY CURRENT vs SUPPLY VOLTAGE

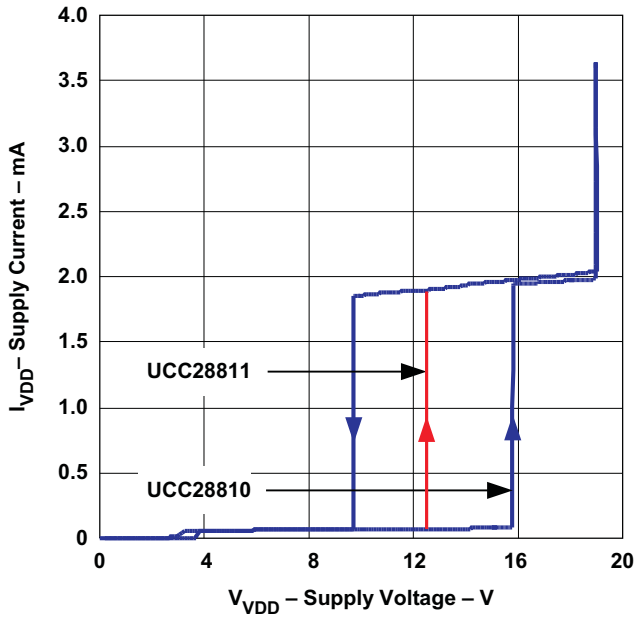


Figure 3.

SUPPLY CURRENT vs JUNCTION TEMPERATURE

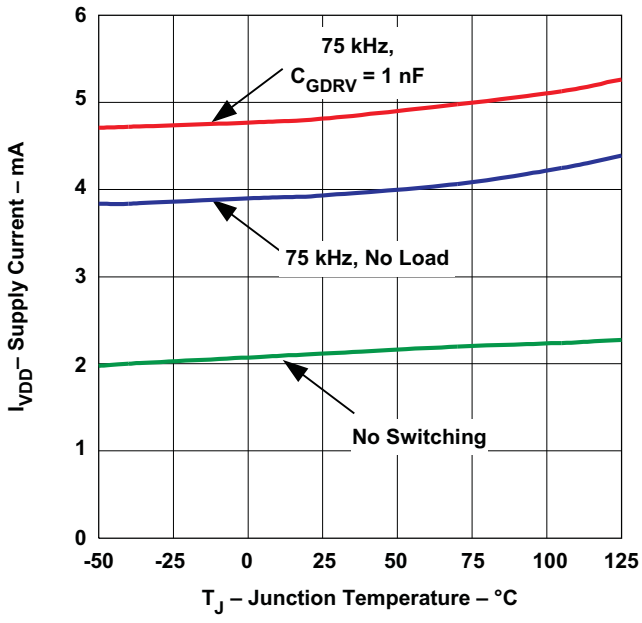


Figure 4.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, V_{VDD}=12 V, –40°C ≤ T_A = T_J ≤ 105°C

UVLO THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

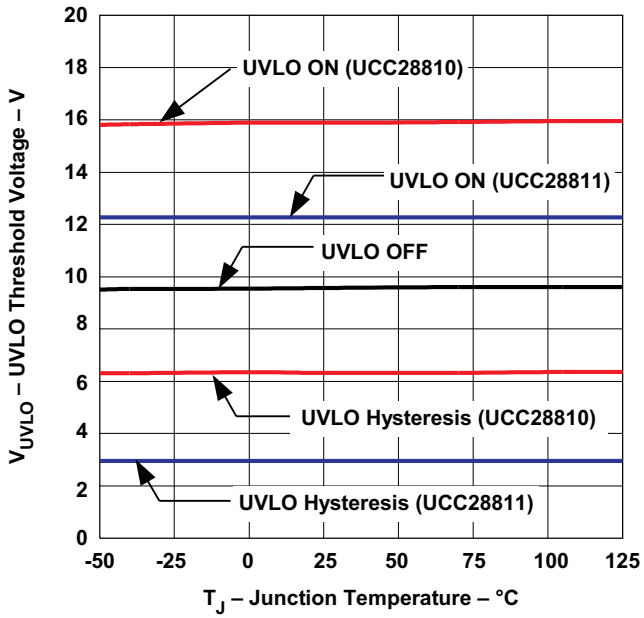


Figure 5.

INTERNAL REFERENCE VOLTAGE
vs
JUNCTION TEMPERATURE

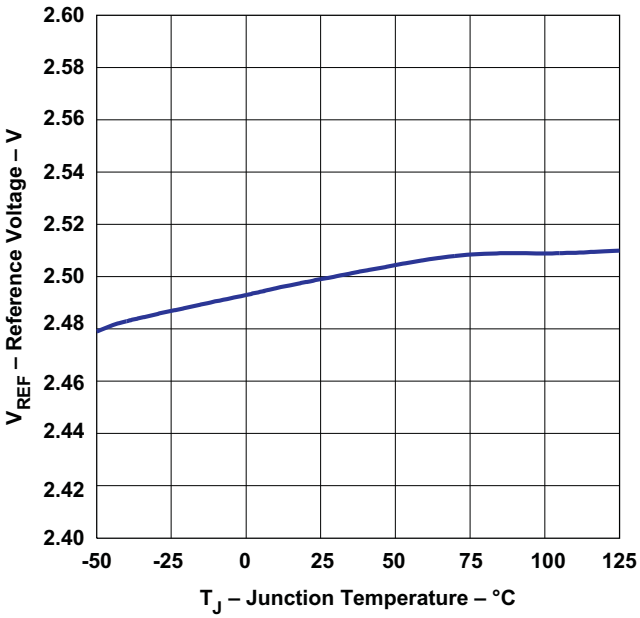


Figure 6.

ISENSE INPUT VOLTAGE
vs
CURRENT REFERENCE GENERATOR INPUT VOLTAGE

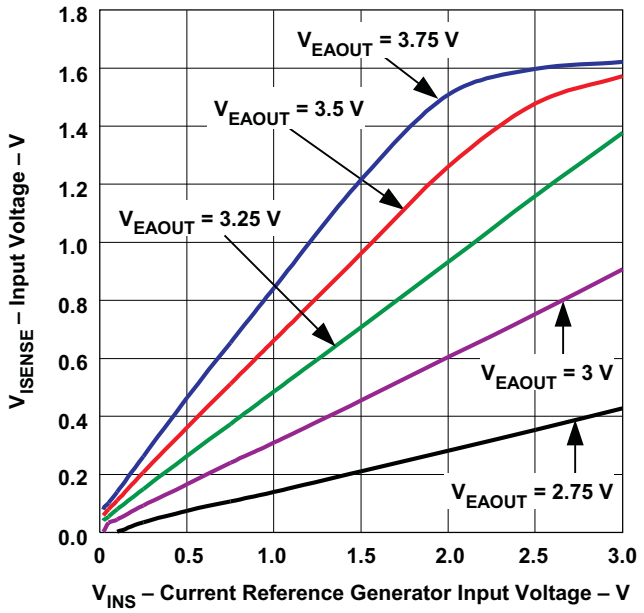


Figure 7.

CURRENT SENSE TO DRIVER DELAY TIME
vs
JUNCTION TEMPERATURE

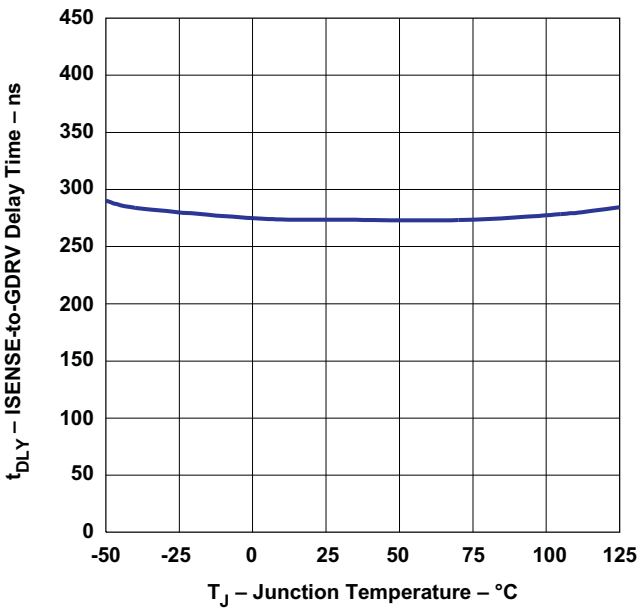


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, V_{VDD}=12 V, –40°C ≤ T_A = T_J ≤ 105°C

TRANSCONDUCTANCE
vs
JUNCTION TEMPERATURE

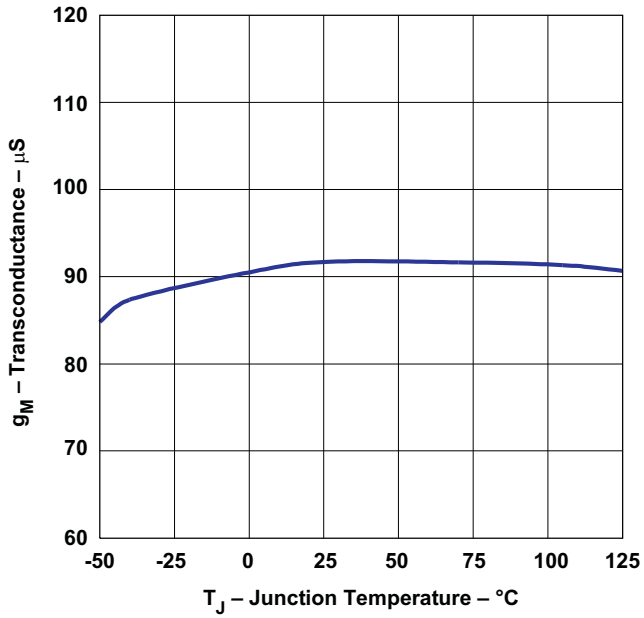


Figure 9.

TRANSCONDUCTANCE AMPLIFIER CURRENT
vs
OUTPUT SENSE VOLTAGE

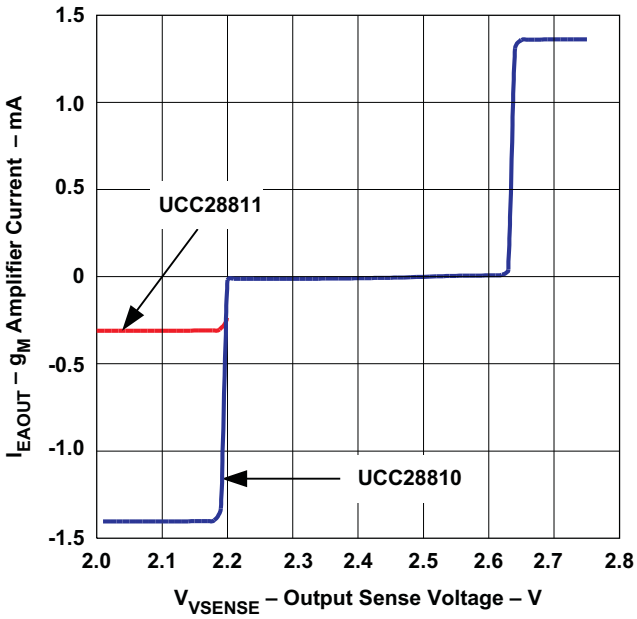


Figure 10.

TRANSCONDUCTANCE AMPLIFIER CURRENT
vs
OUTPUT SENSE VOLTAGE

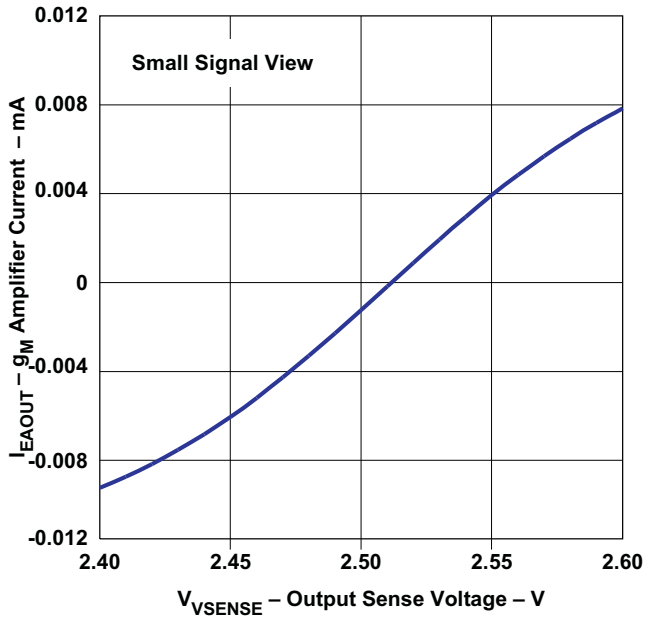


Figure 11.

OVERVOLTAGE PROTECTION THRESHOLD
vs
JUNCTION TEMPERATURE

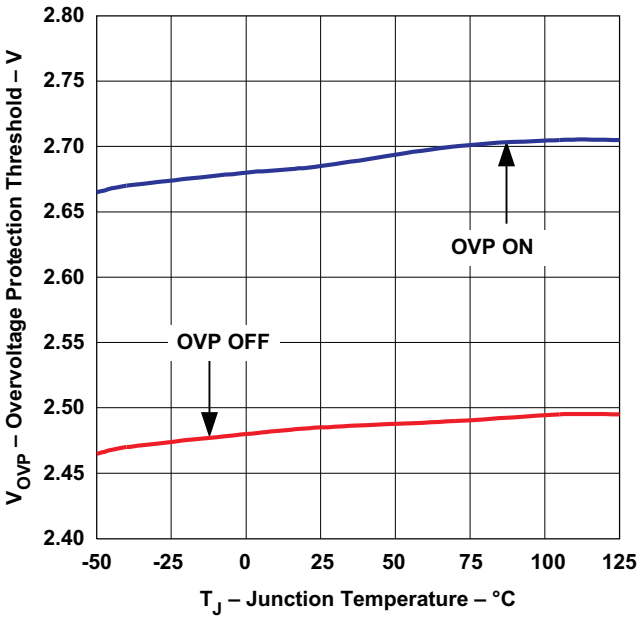


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, V_{VDD}=12 V, –40°C ≤ T_A = T_J ≤ 105°C

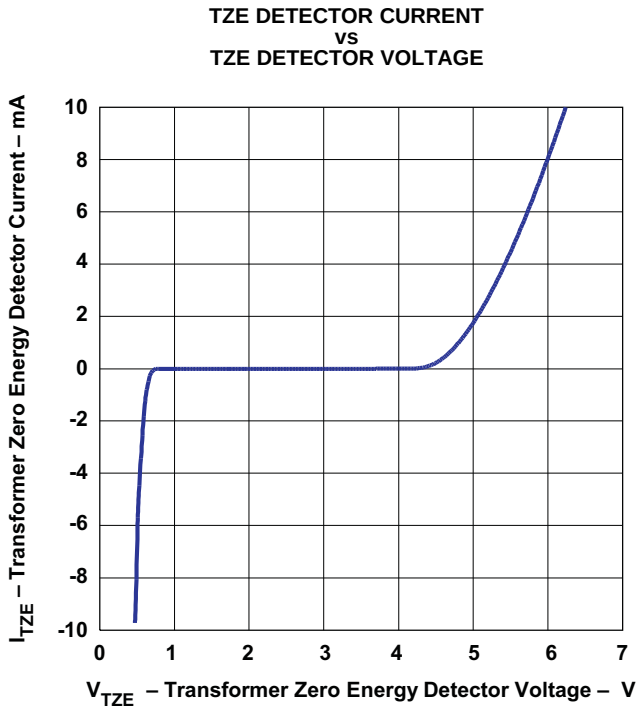


Figure 13.

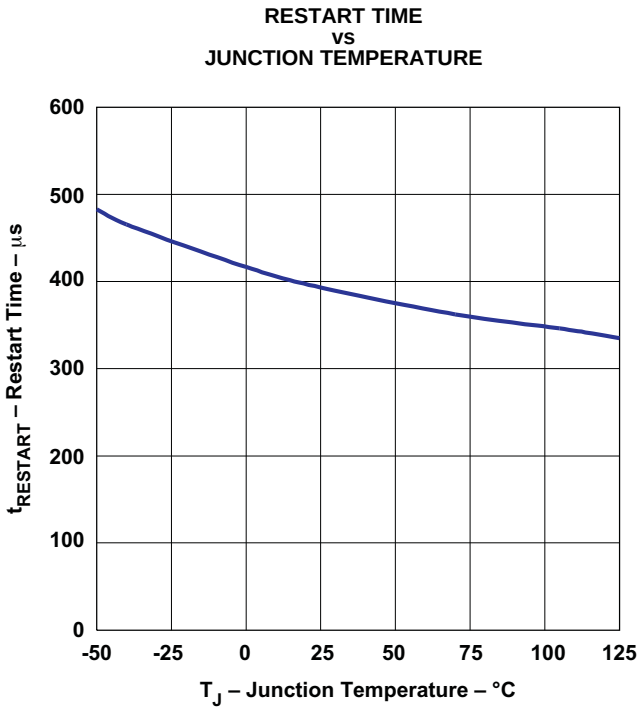


Figure 14.

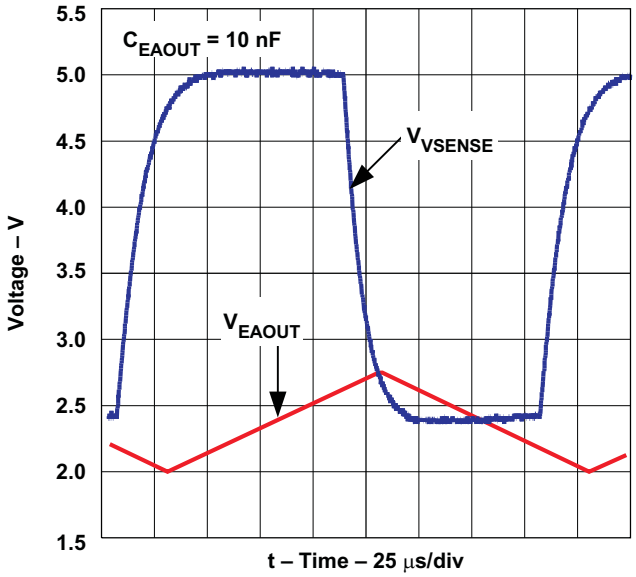


Figure 15. Voltage Amplifier Outputs

REFERENCE DESIGNS

REFERENCE DESIGN 1

Introduction

This reference design, (schematic shown in Figure 16) uses the UCC28810 LED lighting power controller in a 25-W single stage triac dimmable PFC flyback converter. The input accepts a voltage range of 85 VAC to 305 VAC and the output provides a regulated 750-mA current source to drive the LEDs.

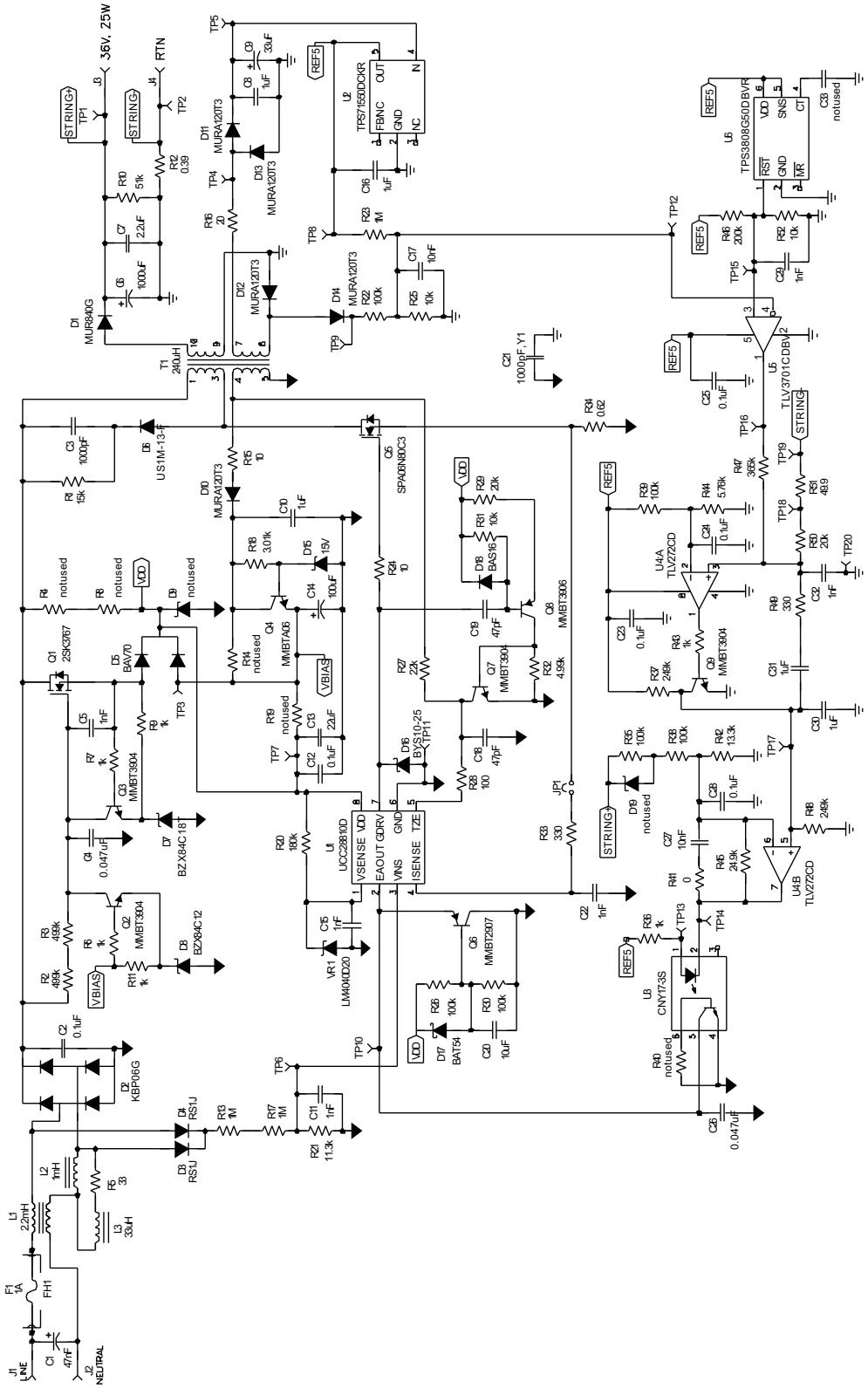


Figure 16. Reference Design 1: 25-W PFC Flyback Converter

THEORY OF OPERATION

Transition Mode Operation

When the primary MOSFET switch is turned on, the drain current ramps from zero to a peak value determined by the current reference generator output, which is the combination of the EAOUT pin voltage and the AC line voltage waveform applied to the VINS pin. The EAOUT pin sets the power level to be transferred to the secondary over the half sinewave cycle, and the current reference generator forces the peak switch current to track the input line voltage to improve the power factor.

When the main switch is turned off, the peak current in the flyback inductor is transferred to the secondary side and flows through the output diode to the output capacitors. This current drops to zero at the rate determined by the output winding inductance and the output capacitor voltage. When the output current reaches zero, the diode stops conducting, and all of the output windings and the drain of the MOSFET ring down towards ground. This ringing is detected on the primary side by the TZE pin of the UCC28810 as it rings below approximately 1.4 V on the bias winding. This triggers the next switch-on pulse to start very near the valley of the ringing waveform on the drain of the FET, which lowers the switching losses due to C_{OSS} and reduces EMI generated by the turn on of the FET

Input Filter Damping Network

Offline flyback converters typically need common mode and differential mode input EMI filters to meet EMI specifications. When a triac dimmer is used with a typical L-C EMI filter, the sharp turn on edge that is generated by the triac phase control causes the LC filter to ring back and set up an oscillation between the triac and the L-C filter. For this reason, the differential part of the filter is damped with a R-L network across the inductor. This can also be accomplished with an R-C damping network across the capacitor. L3 and R5 are the damping components in the schematic shown in Figure 17.

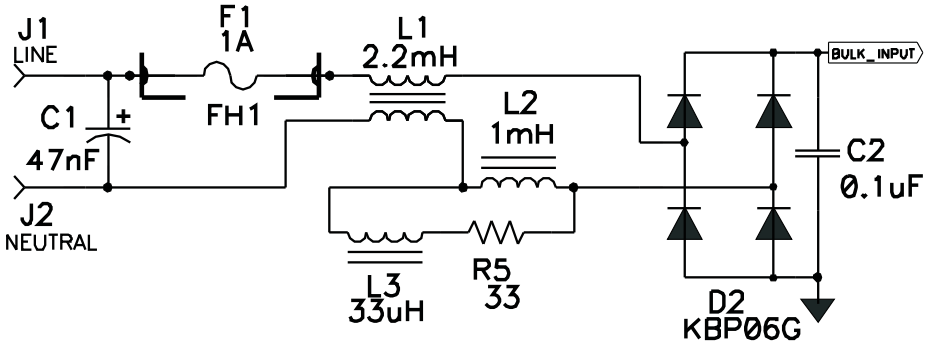


Figure 17. Input Filter Damping Network

High Voltage Startup Circuit

In LED lighting applications it is important that the light source starts quickly after the input power is switched on. In the circuit shown in Figure 18, the FET Q1 is turned on at a rate determined by R2 plus R3 and C4. The source follows the gate as it rises. When the source reaches approximately 18.7 V, Q3 prevents the source from increasing, and the UCC28810 starts. When the supply begins to deliver power to the output, V_{BIAS} is higher than 12.7 V, and Q2 lowers the gate voltage of Q1 to turn off the startup current path and improve efficiency. For single range input supplies, or supplies that can start more slowly, R4, R8, and D9 can be populated to start the supply. However, the power dissipation in normal operation is much higher and reduces the efficiency.

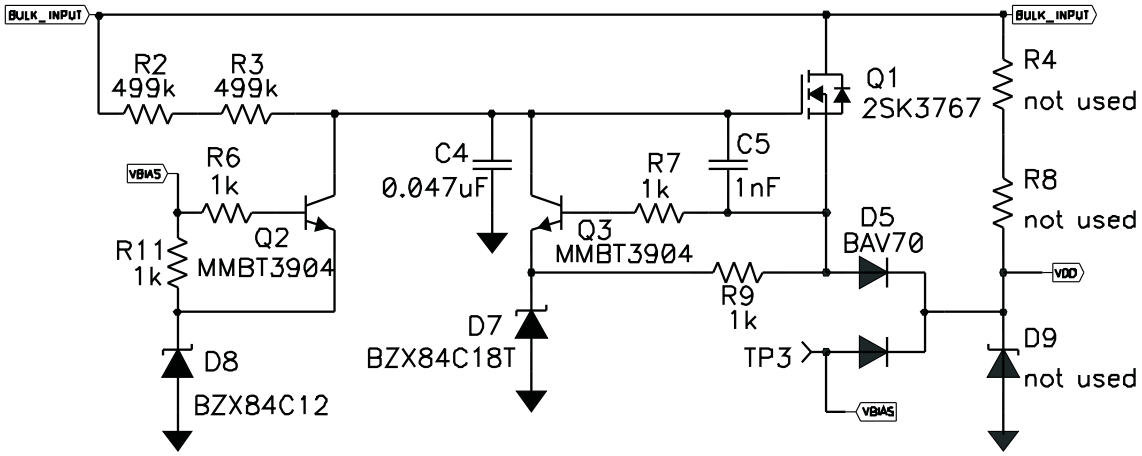


Figure 18. High-Voltage Startup Circuit

Primary-Side Soft Start

The circuit shown in Figure 19 provides an open-loop soft-start that allows the EAOUT pin to slowly rise on the primary side until the secondary-side error amplifier and soft-start function can take over control of the power stage.

When V_{VDD} is applied to the device, C20 is slowly charged to one-half of the voltage on the VDD pin and holds the EAOUT pin to the voltage on C20 plus the V_{BE} of Q6. As the voltage on C20 slowly rises, the EAOUT pin tracks it until the voltage on C20 is above the normal operating point of the EAOUT pin. At some point, the secondary-side error amplifier takes control of the EAOUT pin as it also has a slowly ramping reference that provides a closed-loop soft start.

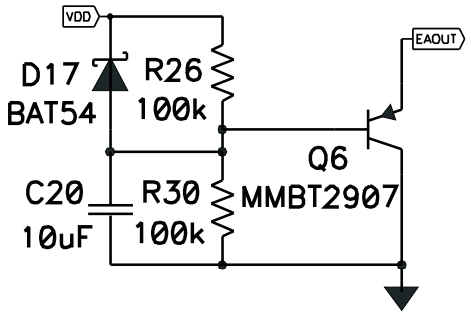


Figure 19. Primary-Side Soft Start

Primary-Side Bias Regulator

The bias for the UCC28810 device is provided by a winding on the flyback inductor that is well coupled to the output winding. When the LED string voltage varies due to dimming or different configurations of LED strings, a primary-side bias regulator formed by D15, R18, and Q4 is needed to limit the range of voltage that is applied to the UCC28810. If dimming is not used, and the LED string forward voltage is well known, then the bias regulator can be removed and R14 can be populated to connect the winding voltage directly to the input supply of the device.

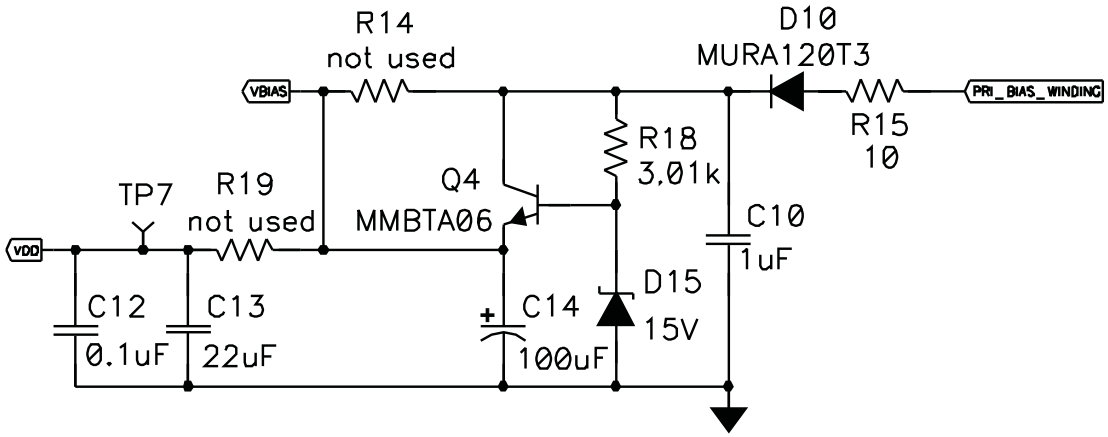


Figure 20. Primary Side Bias Regulator

Leading Edge Blanking Circuit on the TZE Pin

At startup, the output voltage reflected to the bias winding is well below the 1.7-V threshold that allows the next pulse to be triggered by TZE transitioning below 1.4 V. Leakage inductance can occur between the windings causing a leading edge spike on the TZE pin that could potentially trigger the TZE threshold and start the next pulse before the output winding current has reached 0 A. If this happens to several pulses in a row, the primary current continues to increase cycle-by-cycle until the transformer saturates and the MOSFET passes it's safe operating area and is destroyed. The leading edge blanking circuit shown in Figure 21, consists of a charge pump, level shift, and timed blanking pulse. When the GDRV output to the MOSFET gate switches high, C19 is discharged to VDD through D18. When the GDRV output transitions low, the base of Q8 is pulled down, and a timer consisting of C19 and R31 is started.

For the time allowed, current set by R29 is fed through Q8 to the base of Q7, which pulls the TZE pin to GND. Because the TZE pin sources current at approximately 0.5 V, a 100-Ω resistor, R28, is used to limit the current and to allow C18 to be pulled below the TZE clamp by saturating Q7. When the time expires (approximately 1 µs in the schematic shown in Figure 21) C18 is charged by R27 to the bias winding voltage. When this voltage charges above 1.7 V, the PWM latch is ready to be set by the TZE pin falling below 1.4 V, and the leakage inductance spike has been effectively blanked. When the pulse width is very small, it is possible that the time set by the blanking circuit is longer than the secondary conduction time. When this happens, the next oscillation of the winding is detected and the valley causes the main switch to fire. If no falling edge is detected, or the TZE pin never rises above 1.7 V, then a 400-µs timer triggers a new pulse.

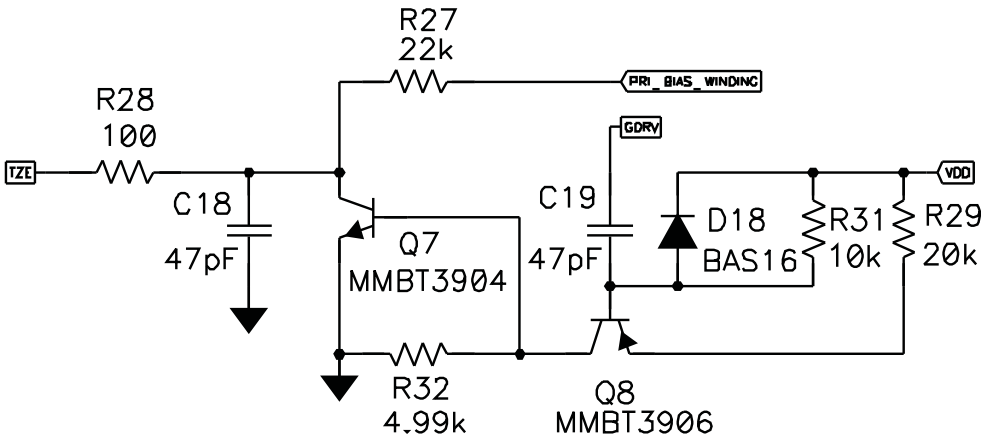


Figure 21. Leading Edge Blanking Circuit on TZE

Secondary Bias Regulator

Normally, only D11 is needed for a secondary bias supply to charge the bias capacitor, C9, during the switch-on time, based on the turns ratio between the output and bias winding. U2 provides a stable 5-V bias for the secondary-side circuitry. For this application, D12, D13, D14 are added to provide a copy of the input voltage on the secondary side during the switch on time. This input waveform is divided down and filtered to remove the switching frequency waveform by R22, R25, and C17. The signal is then offset by R23 and fed into a comparator, U5, shown in Figure 23, to detect triac dimming and adjust the feedback loop.

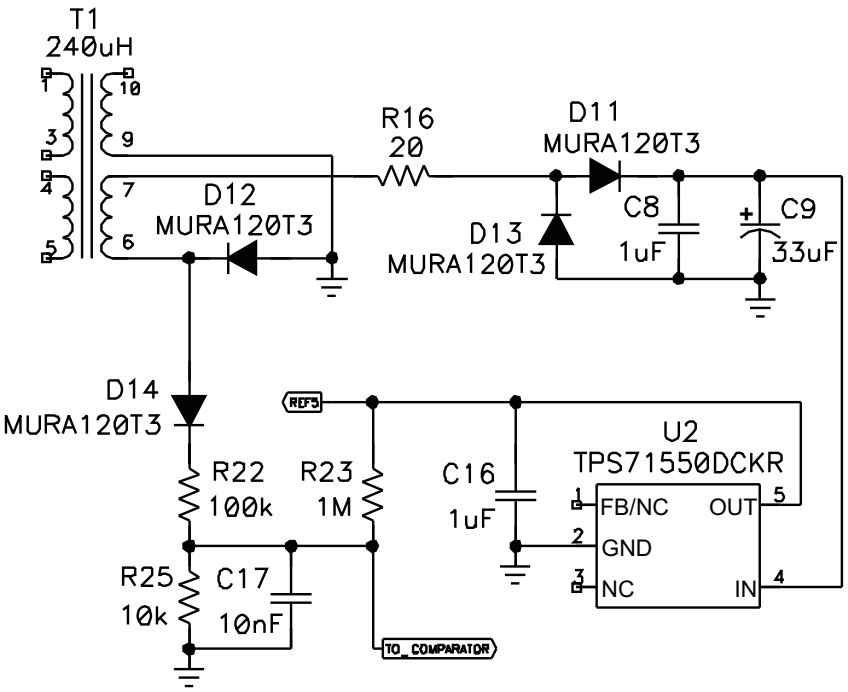


Figure 22. Secondary Bias Regulator Schematic

Triac Dimming Detection Circuit

The comparator U5 compares the copied input voltage waveform to a fixed threshold, and emits a positive pulse any time the input waveform is detected to be below the threshold. This results in a small pulse at every zero crossing in normal operation. When a triac dimmer is used, the pulse width matches the triac dimmer off-time. This pulse sums in to the current-sense error amplifier and reduces the current regulated in the string proportional to the off time of the triac. The programmable delay supervisory component, U6, blanks the dimming at startup and allows the converter to start properly.

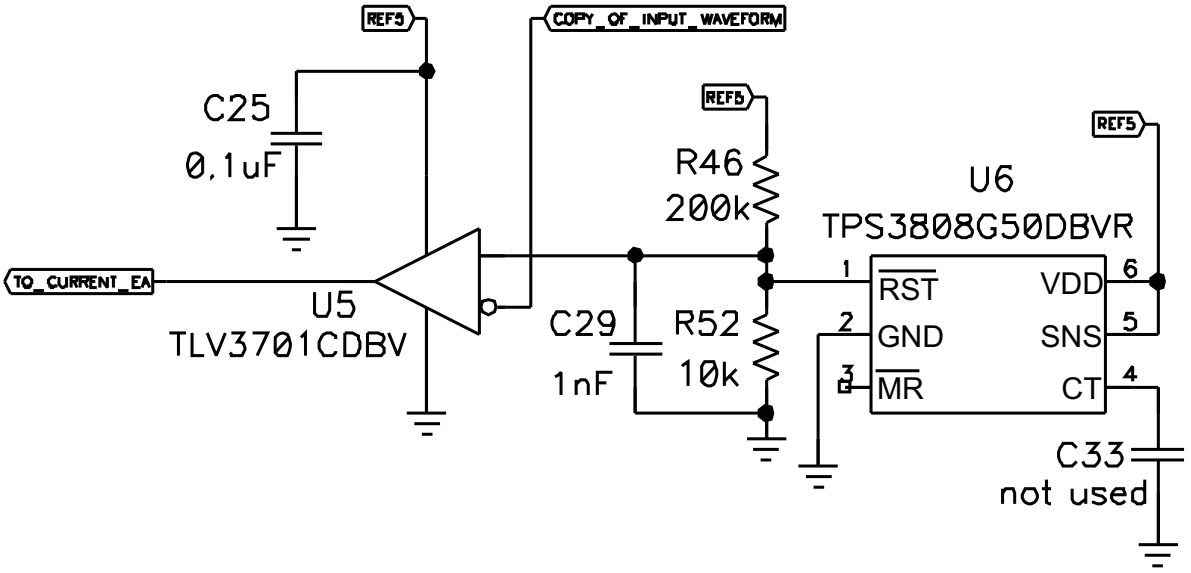


Figure 23. Triac Dimming Detection Circuit

Current Error Amplifier, Soft-Start, and Voltage Limit Amplifier

Component U4A, shown in Figure 24, fulfills the function of current error amplifier in this application.. A fixed threshold is set by R39 and R44 and the current on the sense resistor, as represented by the signal from the triac dimmer detection circuit, is compared to this voltage by U4A. R47 sums in the PWM dimming signal from the triac dimming comparator. The voltage divider formed by R37 and R48 provides a maximum output of 2.5 V, and the transistor Q9 reduces the voltage at the non-inverting input of the TLV272 to regulate the current in the LED string.

When the supply is starting up, C30 and C31 provide a soft start set by the divider resistance and capacitance value. After the primary soft start charges up, this secondary closed-loop soft start takes control and prevents overshoot of the supply at startup. The soft-start time provided by the secondary soft start should be longer than the time it takes for the power stage to fully charge the output capacitors, so that overshoot does not occur.

The second comparator of the TLV272 component, shown as U4B in Figure 24, provides a voltage limit. Because the voltage at the non-inverting input of the TLV272 cannot go higher than 2.5 V, U4B can provide an effective maximum voltage limit by increasing the LED current in the optocoupler when the voltage is moving through a range determined by R35, R38, and R42. The gain is set by R45, and C27 ensures stability on the amplifier. The voltage limit amplifier is not an integrator, it has a fixed gain. Two integrators in series would cause stability issues due to phase shift. R41 is provided as a provision for disconnecting the current error amplifier and regulating output voltage if desired. R49 and Q9 could be depopulated, and R41 and C27 could be changed to make a voltage error amplifier that is an integrator.

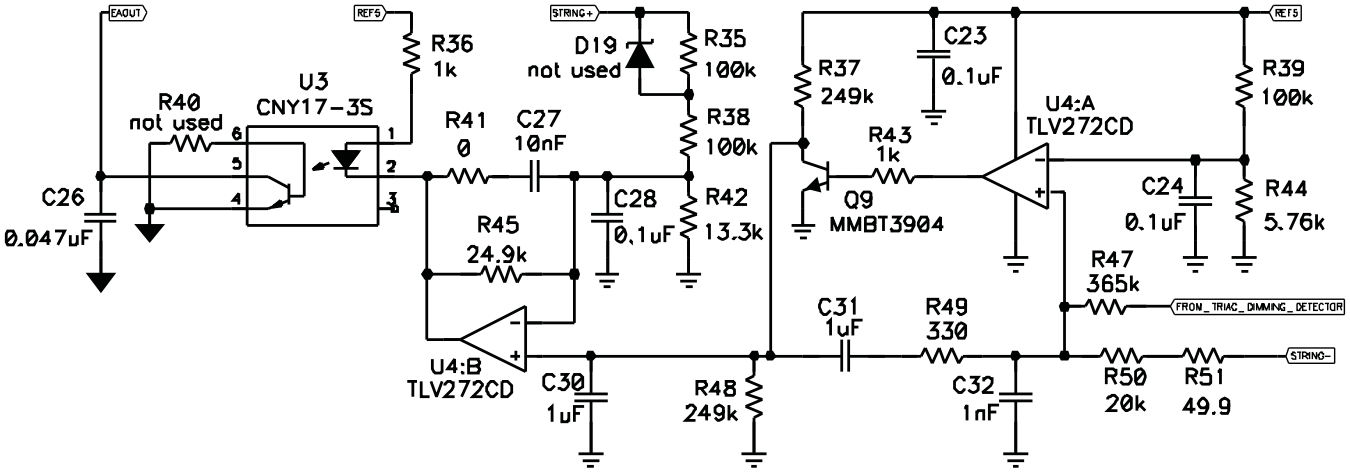


Figure 24. Current Error Amplifier, Soft-Start, and Voltage Limit Amplifier

REFERENCE DESIGN 2

The PR788, shown in Figure 26 is a 100-W offline AC-to-DC LED current driver with power factor correction. This design is a two stage converter design with a universal input boost follower PFC stage providing a 240-V to 400-V DC output and a low-side buck stage providing the current source to power the LEDs. This converter was designed to support up to 30 high-brightness LEDs in series with up to 900-mA average current. The design incorporates an interface for microprocessor control to allow for shutdown into a low power mode (< 0.5 W) and PWM dimming of the LEDs.

PFC Stage

The PFC stage is a critical conduction mode boost converter with a boost follower feature implemented. The boost follower is set to provide a DC output of 240 V_{DC} to 400 V_{DC}. The lower DC output at low input voltage results in improved efficiency at low-line conditions. The minimum regulation point was set at 240 V to allow the design to be scaled to power up to 50 LEDs in series.

The critical conduction mode (CRM) of operation offers advantages regarding losses over continuous conduction mode. In CRM operation, since the inductor current reaches zero just before the beginning of the next cycle, the boost diode reverse recovery loss is eliminated. Switching losses in the MOSFET are reduced as well by programming a small delay after the inductor current reaches 0 A until the turn on of the MOSFET on the next cycle. The voltage across the boost inductor begins discontinuous mode self oscillation which reduces the MOSFET drain voltage at turn on, this delay is optimized to occur at the valley of the first self oscillation cycle.

In the PFC boost implementation, the controller programs the peak inductor current to twice the value of the desired average line current. The current reference generator uses the VINS input and the EAOUT input to program the peak current of the boost inductor. The VINS input is a divided sample of the rectified AC input voltage which is determined by R9 and the sum of (R2 + R5), as shown in Figure 26.

The C6 capacitor is used for high frequency bypass and should not affect the line frequency signal on VINS. The minimum boost output voltage is determined by the feedback divider consisting of R11 and (R13 + R15) connected to the VSENSE pin. The boost follower circuit is hown in Figure 25.The boost follower function is accomplished by Q1 sinking current through the high side of the feedback divider (R13 + R15). The AC input rectified voltage is filtered and divided by R1, R3, R4, and C3. Ideally the filter minimizes the line frequency ripple and generates a DC sample of the RMS input voltage. The ratio of R4 and (R1 + R3) determines the line voltage which Q1 begins increasing the output by sinking current thru R13 and R15. R7 is determined by

1. determining the current through R13 and R15 that provides the desired increase in the boost output
2. determine the voltage across R4 at high line

$$R7 = \frac{V_{R4} - V_{BE}}{I_{R15}} \quad (1)$$

.

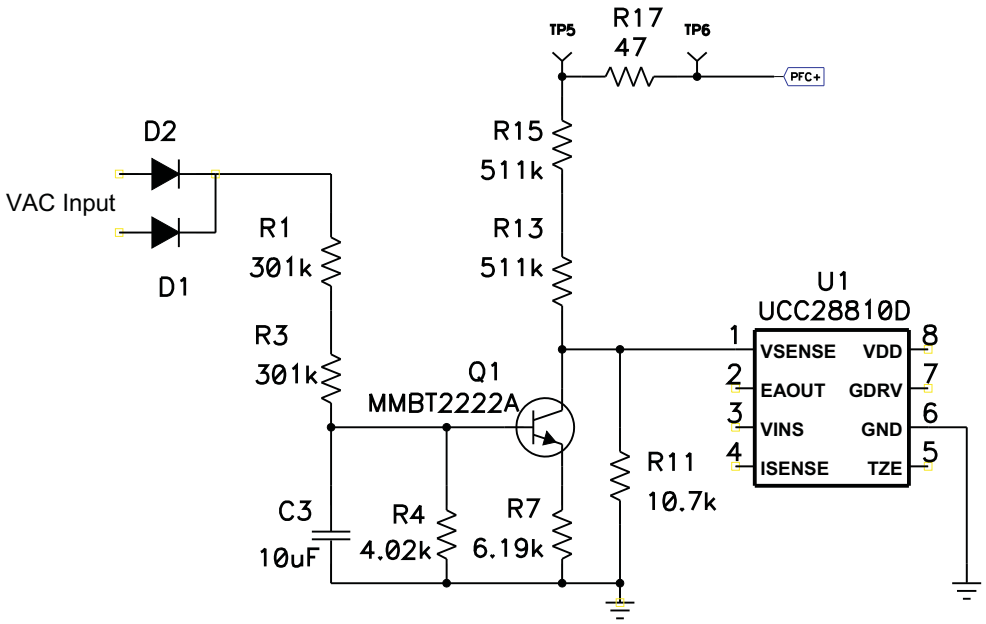


Figure 25. Boost Follower Circuit

The voltage error amplifier compensation network is R10, C4 and C7 connected from EAOUT to GND. The goal is to provide a loop crossover frequency at 1/10 input line frequency (10 Hz) with 45° phase margin.

The current sense resistor (R21) is determined by the following equation which is based on peak inductor current at low line, 1.7 V ISENSE threshold, and 20% margin.

$$R21 \cong \frac{1.7\,V}{\frac{P_{OUT} \times 2 \times \sqrt{2} \times 1.2}{\eta \times V_{IN(min)}}} \tag{2}$$

The boost inductor value can be determined based on the desired minimum operating frequency which occurs at the peak of low line input voltage.

$$L2 \cong \frac{\left(V_{OUT(min)} - \sqrt{2} \times V_{IN(min)}\right) \times \eta \times \left(V_{IN(min)}\right)^2}{2 \times f_S \times V_{OUT(min)} \times P_{OUT}} \tag{3}$$

.

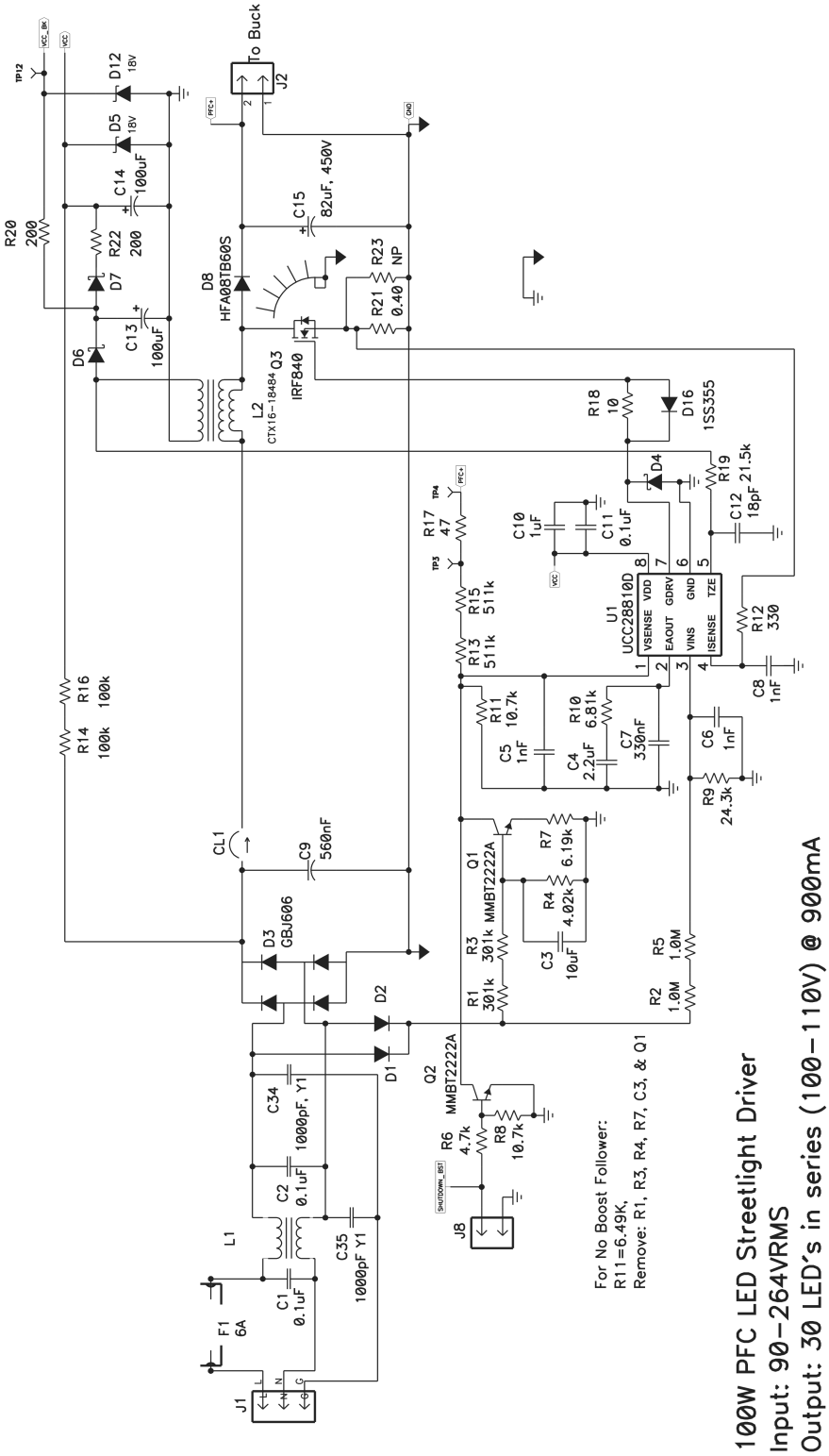


Figure 26. PR788 Reference Design Schematic

Low-Side Buck Stage

The LED current is provided by a low-side buck converter operating in critical conduction mode, shown in Figure 29. The buck controller is programmed to provide a peak current of two times (2 ×) the maximum average load current of 0.9 A (nom). The critical conduction mode allows the current to reach 0 A before beginning the next cycle. This method provides high-efficiency due to minimized voltage on the MOSFET drain at turn on. Cycle-by-cycle current control to the LEDs is also a benefit of critical conduction mode. The average current of the buck driver is controlled via the PWM input (J9, Pin 3).

The UCC28811 is configured to operate in peak current limit mode with the ability to shutdown and PWM control the buck converter with the enable function on the VSENSE pin.

The voltage divider formed by R27 and R28 from the 5.1-V zener diode (D9) provides approx 2 V to VSENSE which is below the internal reference and above the enable threshold. R29 and R30 is a divider which biases VINS at approx 3 V.

The saturated EAOUT and VINS saturates the current reference generator so the UCC28811 VDRV termination is determined by 1.7 V on ISENSE. R_{SENSE} (R36 + R38) is determined by the current sense threshold and 2 times the desired average LED current

The minimum operating frequency of a given inductor value can be determined by summing the on and off time of the buck switch to achieve the desired peak-to-peak current.

$$f_{SW(min)} \cong \frac{1}{\left(\frac{L \times I_{PK}}{V_{IN} - V_{OUT}}\right) + \left(\frac{L \times I_{PK}}{V_{OUT}}\right)} \tag{4}$$

R40 and R48 provide a small current from LED+ into the ISENSE filter to offset the change in peak current due to the propagation delay of the ISENSE comparator. The change in di/dt from minimum to maximum V_{LED+} is determined. The delta in di/dt results in a ΔV across R_{SENSE} (R36 + R38). R40 and 48 are sized to match this ΔV across (R36 + R37 + R38) with the current developed by $V_{LED+(max)}$–$V_{LED+(min)}$.

Overvoltage protection is provided to protect against open circuit loads, shown in Figure 27. The circuit provides detection of voltage between LED+ and LED– without a current path from LED- to ground in normal operation. The trigger voltage is determined by the total zener voltage of D15 and D19, (150 V) in this example. Once the zener breakdown is exceeded, the current through R43 will forward bias the V_{BE} of Q6. The collector voltage of Q6 is divided down with R44 and R42 and summed into the buck shutdown through D14.

A undervoltage lockout circuit is recommended for low-side buck LED current sources operating at output voltages over 115 V. A simple, effective UVLO circuit is shown in Figure 28. When the 2N2222 transistor is off, the collector is pulled high which disables the buck convertor through the common shutdown path . When the total zener voltage is exceeded, the 2N2222 is turned on enabling the buck converter. The UVLO enable voltage should be selected to be between the highest anticipated buck output and the minimum output voltage of the PFC boost follower.

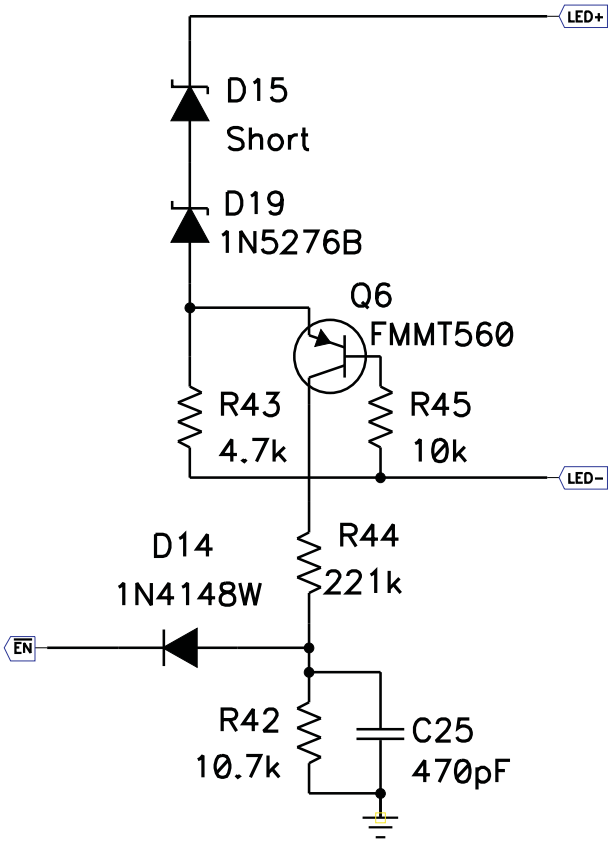


Figure 27. Low-Side Buck OV Protection Circuit

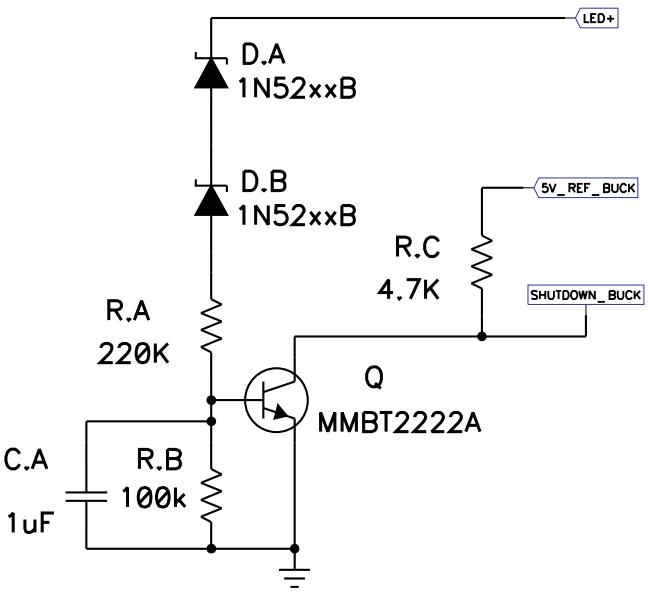


Figure 28. Low-Side Buck UVLO Circuit

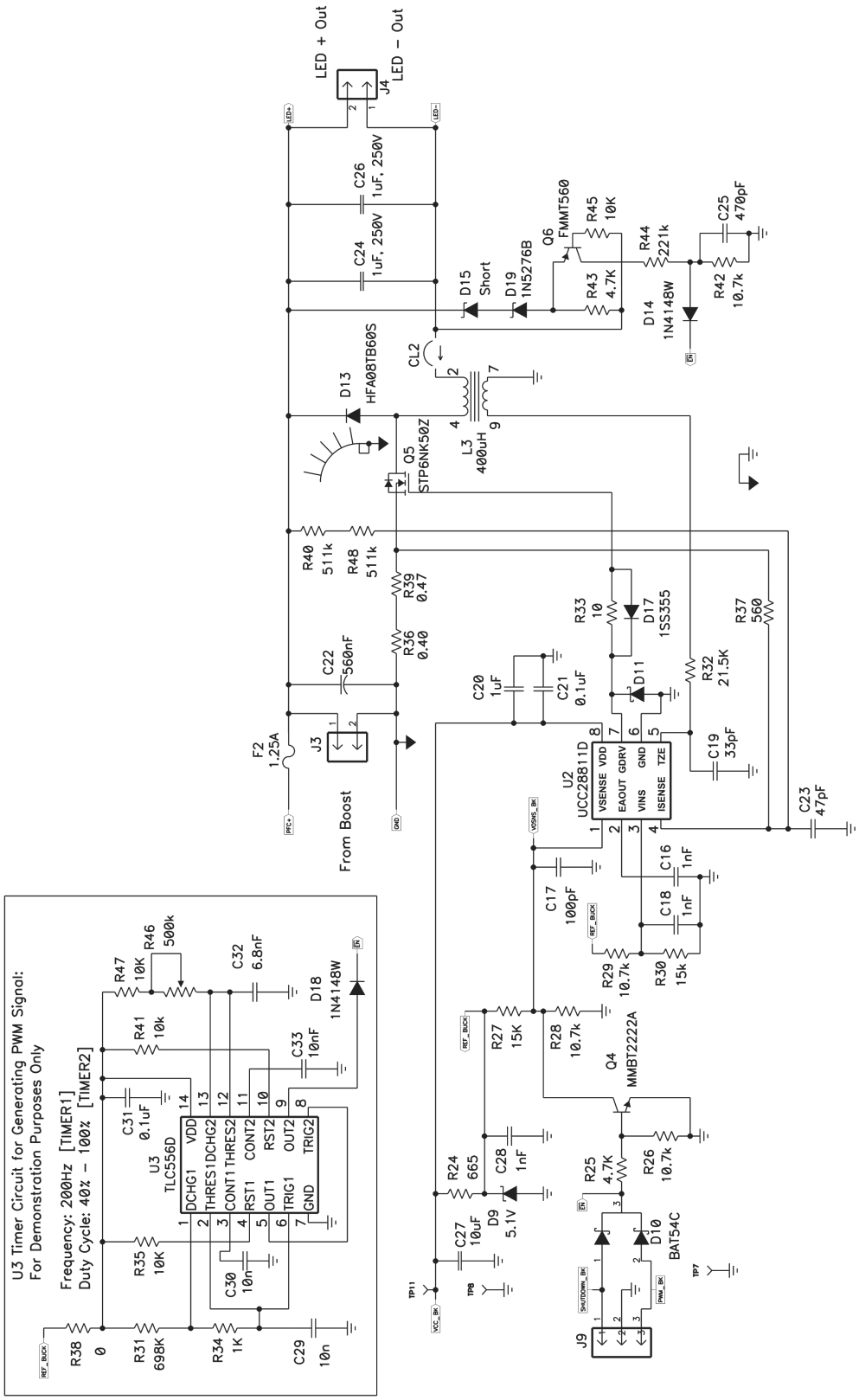


Figure 29. Low-Side Buck Converter Operating in CCM

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	O
UCC28810D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	
UCC28810DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	
UCC28810DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	
UCC28810DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	
UCC28811D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	
UCC28811DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including t
do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in sp
reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm
flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a lin
of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/B
lines if the finish value exceeds the maximum column width.

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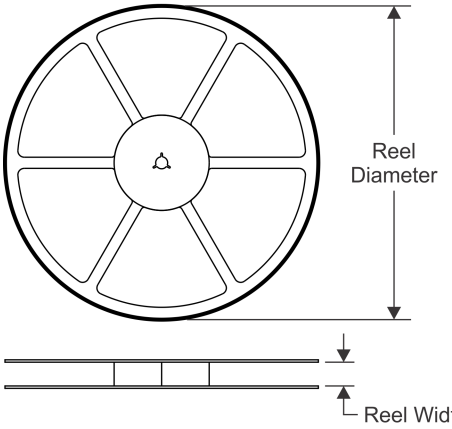
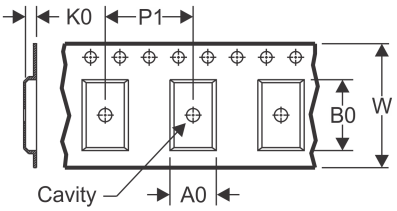
TAPE AND REEL INFORMATION

REEL DIMENSIONS

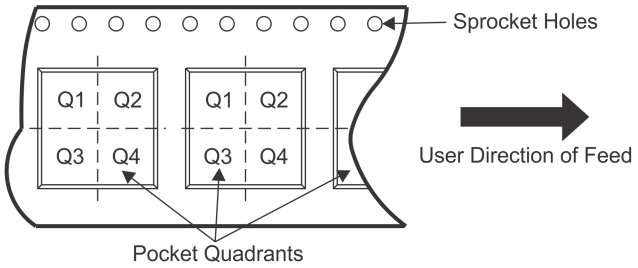


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

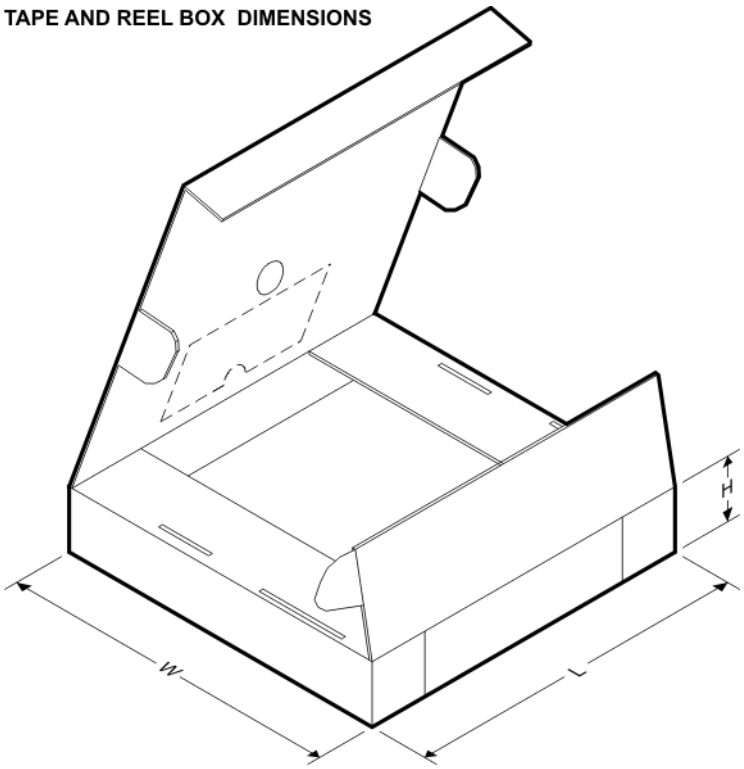
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28810DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28811DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

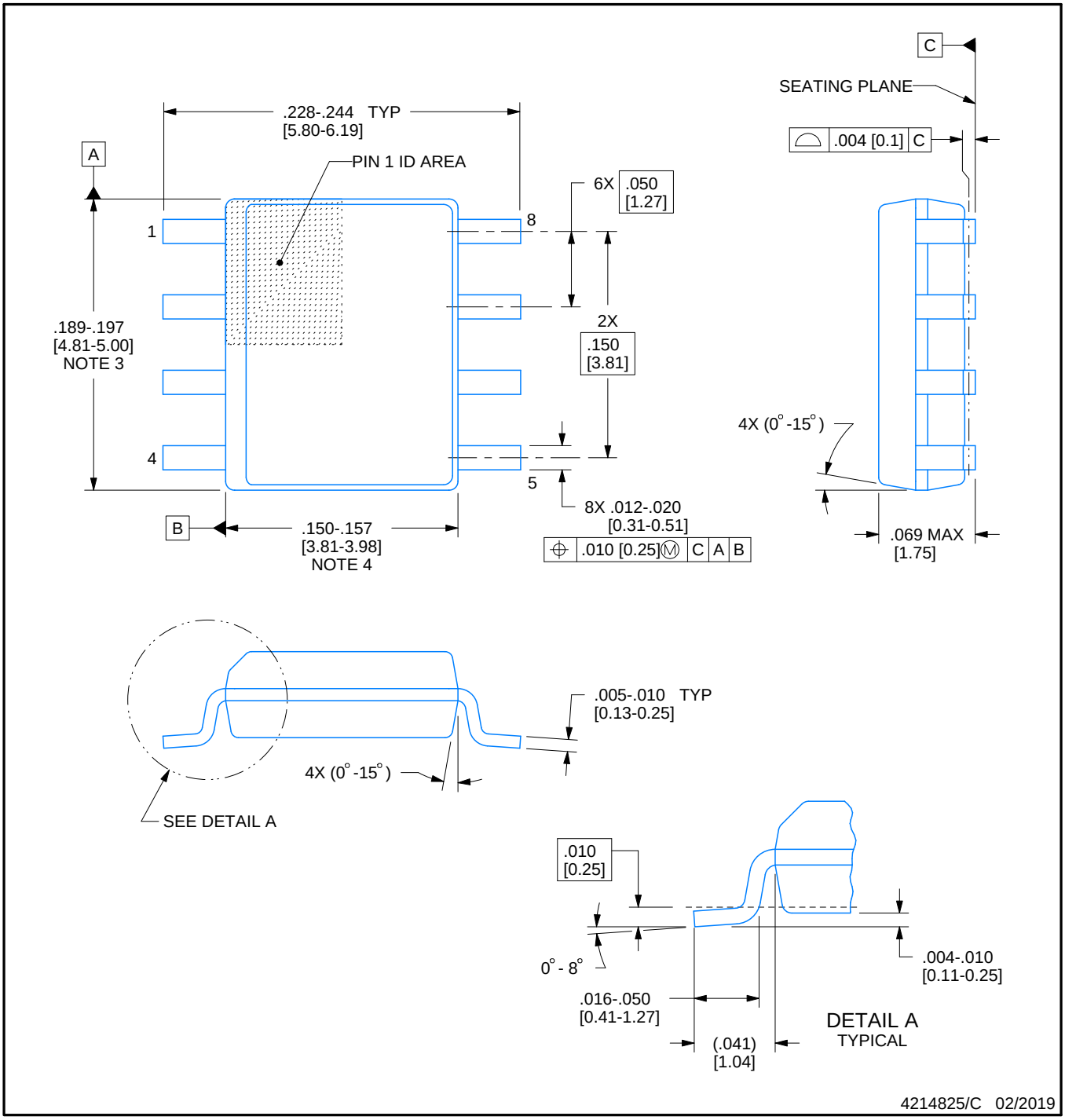
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28810DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC28811DR	SOIC	D	8	2500	340.5	338.1	20.6

PACKAGE OUTLINE

D0008A

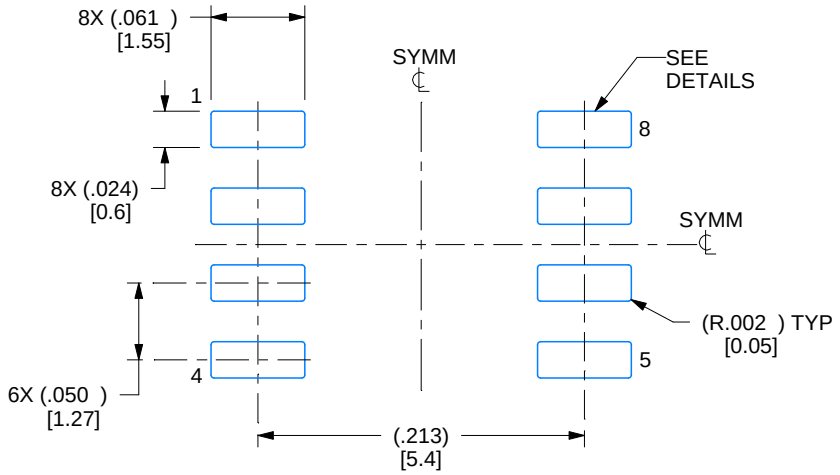
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

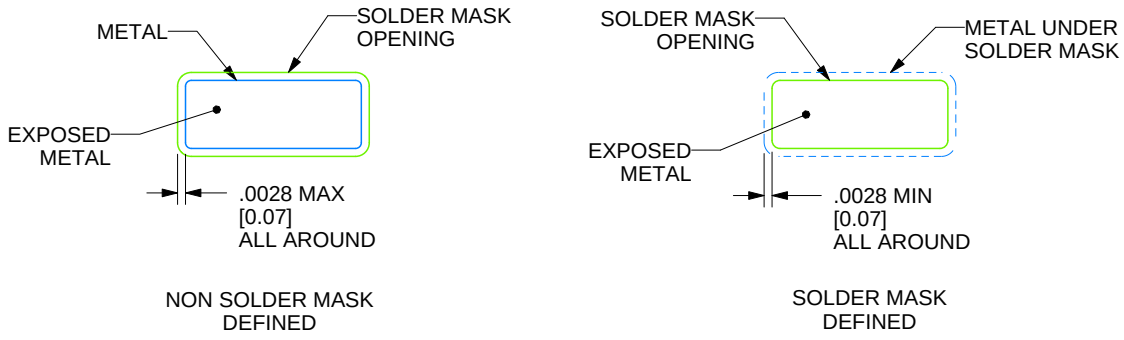


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

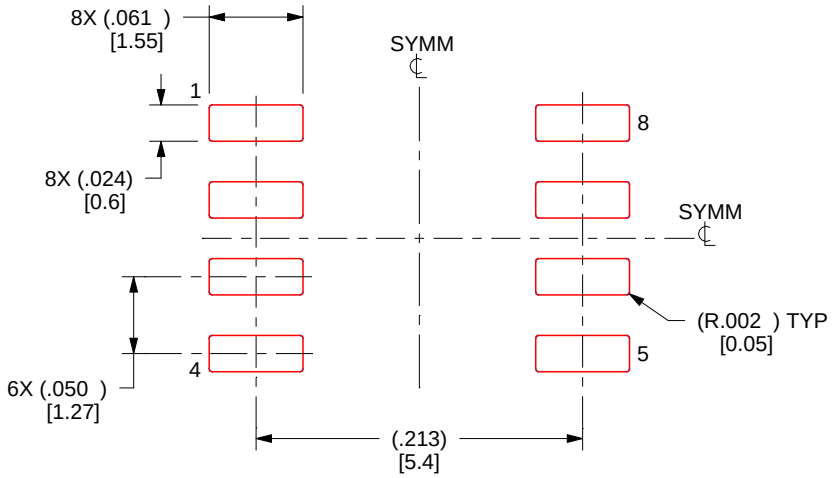
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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