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# BSC032N04LS

Infineon Technologies

MOSFET DIFFERENTIATED MOSFETS

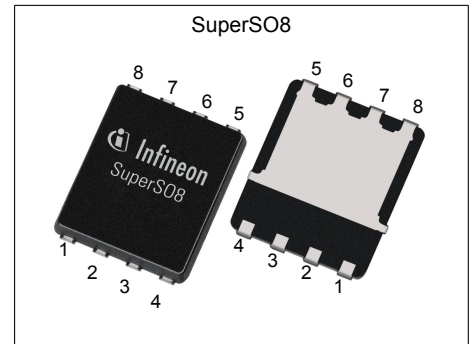
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# MOSFET

## OptiMOS™ Power-MOSFET, 40 V

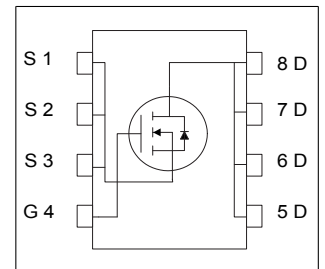
### Features

- Optimized for high performance SMPS, e.g. sync. rec.
- Very low on-resistance  $R_{DS(on)}$  @  $V_{GS}=4.5\text{ V}$
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	40	V
$R_{DS(on),max}$	3.2	mΩ
$I_D$	98	A
$Q_{OSS}$	22	nC
$Q_G(0V..10V)$	25	nC



Type / Ordering Code	Package	Marking	Related Links
BSC032N04LS	PG-TDSON-8	032N04LS	-

<sup>1)</sup> J-STD20 and JESD22

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	98	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=4.5\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}^1)$
		-	-	62		
		-	-	83		
		-	-	53		
		-	-	21		
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	392	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>3)</sup>	$E_{AS}$	-	-	30	mJ	$I_D=40\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	52	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}^1)$
		-	-	2.5		
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	1.4	2.4	K/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>1)</sup>	$R_{thJA}$	-	-	50	K/W	-

<sup>1)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>2)</sup> See Diagram 3 for more detailed information

<sup>3)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	$V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.5 3.3	3.2 4.4	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ $V_{GS}=4.5\text{ V}$ , $I_D=50\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	0.8	1.6	$\Omega$	-
Transconductance	$g_{fs}$	75	150	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=50\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	1800	2520	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=20\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	500	700	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=20\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	40	80	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=20\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	4	-	ns	$V_{DD}=20\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	4	-	ns	$V_{DD}=20\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	19	-	ns	$V_{DD}=20\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	3	-	ns	$V_{DD}=20\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	4.8	-	nC	$V_{DD}=20\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	2.8	-	nC	$V_{DD}=20\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	4.1	5.7	nC	$V_{DD}=20\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	6.0	-	nC	$V_{DD}=20\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	25	35	nC	$V_{DD}=20\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.7	-	V	$V_{DD}=20\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	13	18	nC	$V_{DD}=20\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	10	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	22	31	nC	$V_{DD}=20\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	52	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	392	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.88	1	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	23	46	ns	$V_R=20\text{ V}, I_F=50\text{ A}, di_F/dt=400\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$	-	52	-	nC	$V_R=20\text{ V}, I_F=50\text{ A}, di_F/dt=400\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test

### 4 Electrical characteristics diagrams

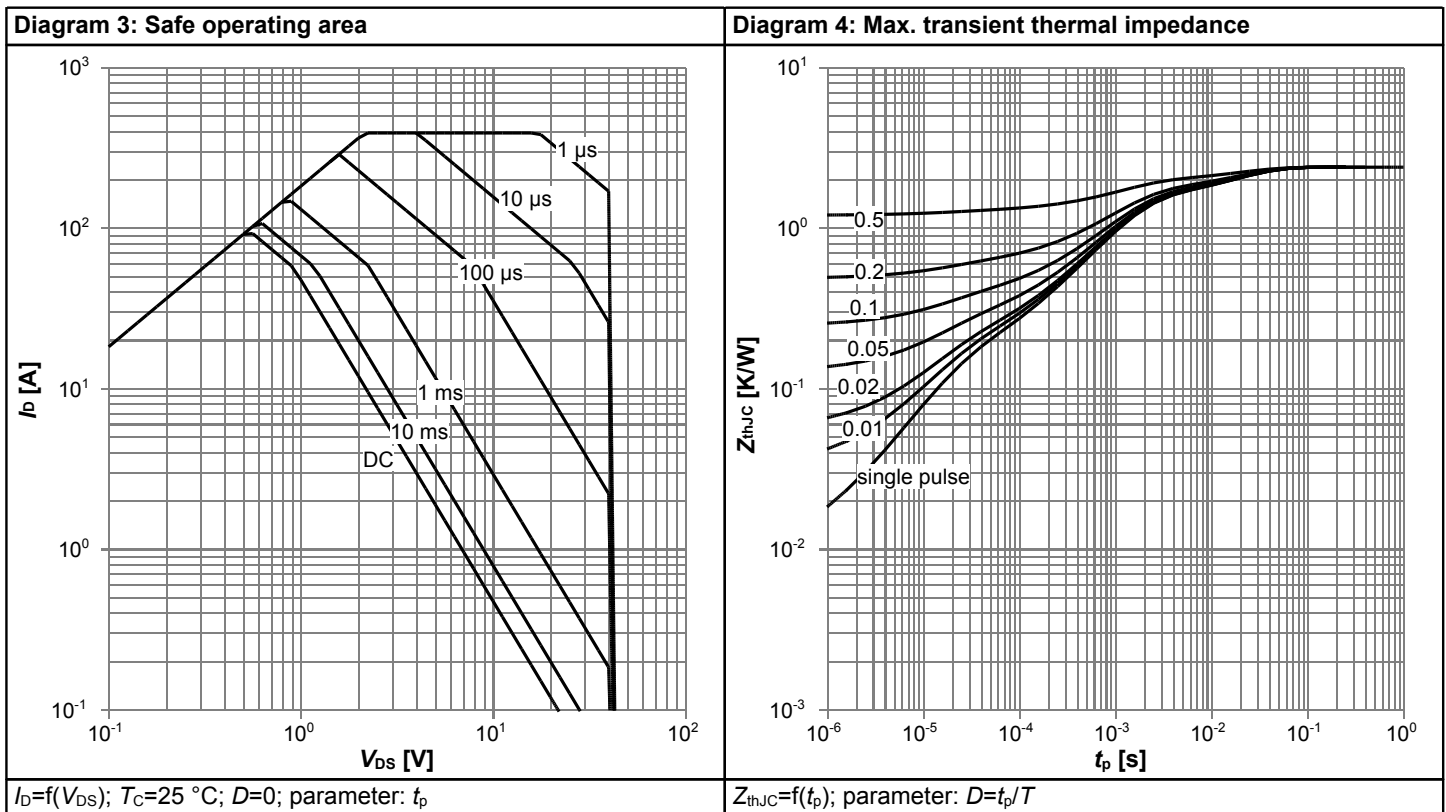
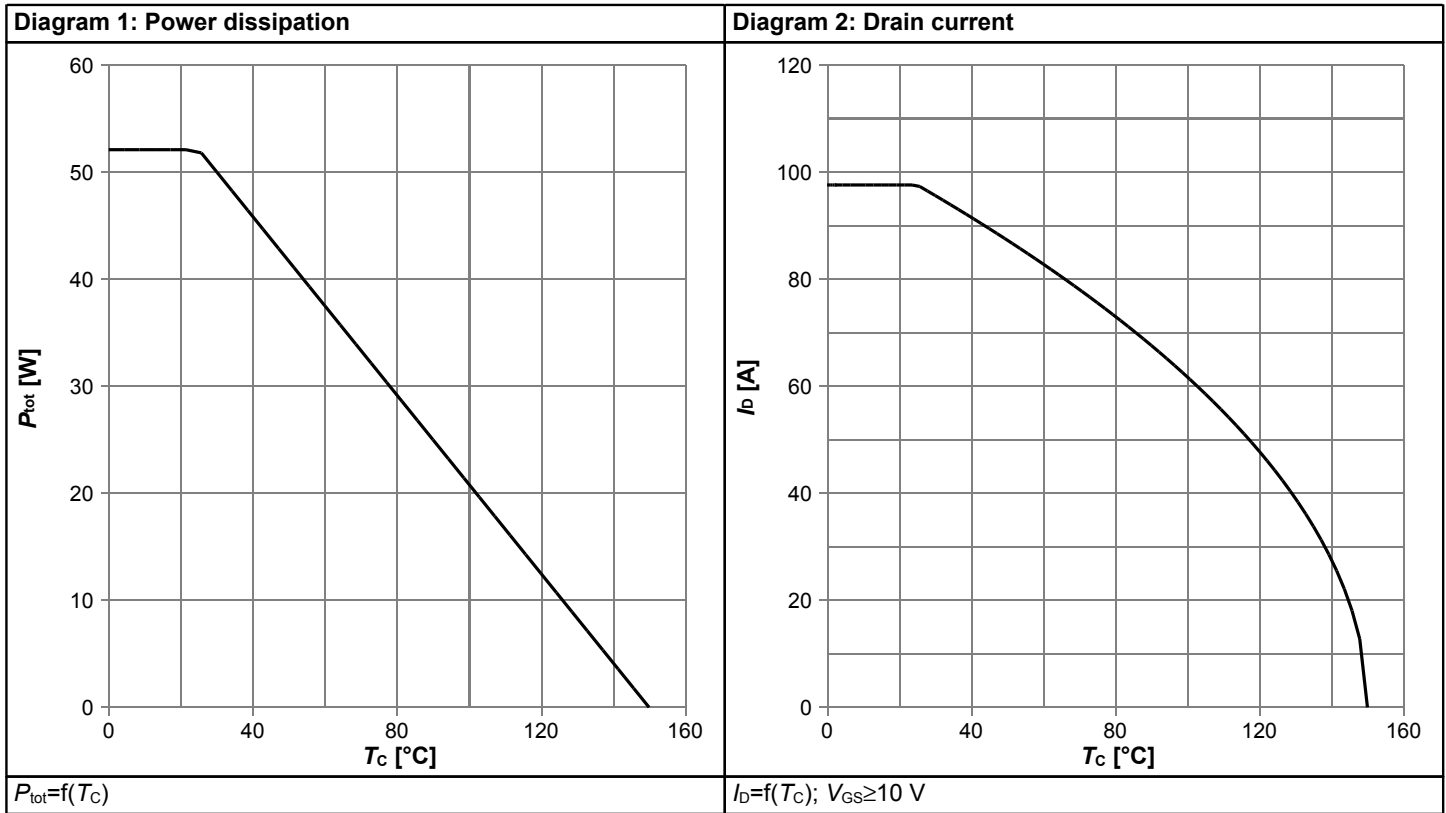
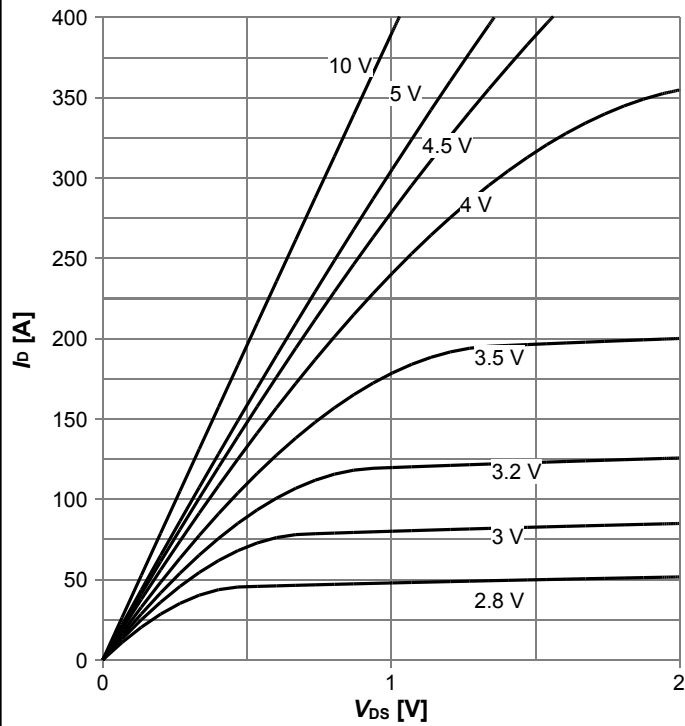
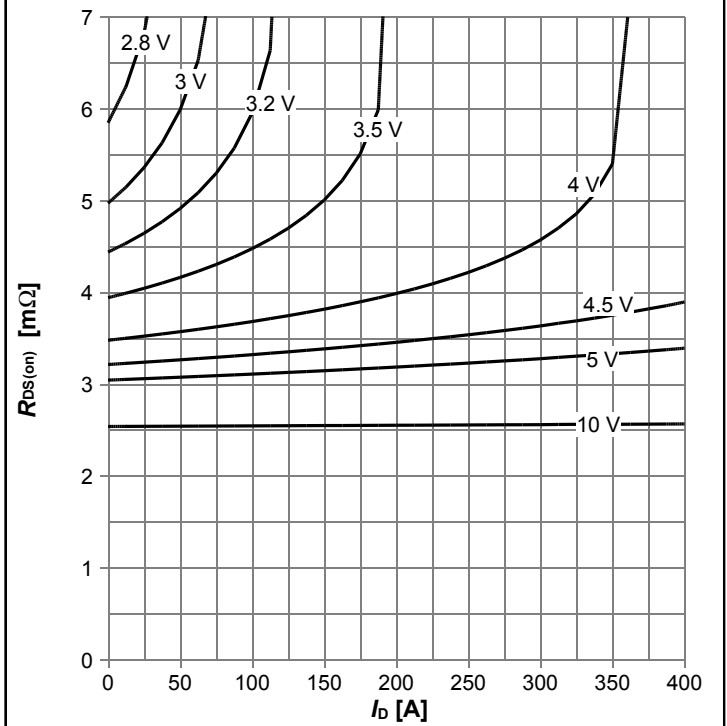


Diagram 5: Typ. output characteristics



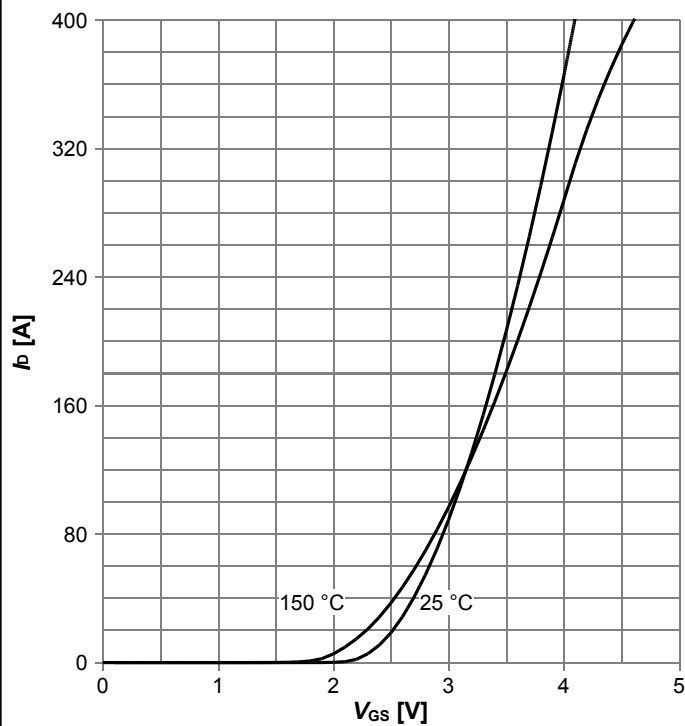
$I_D = f(V_{DS})$ ;  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



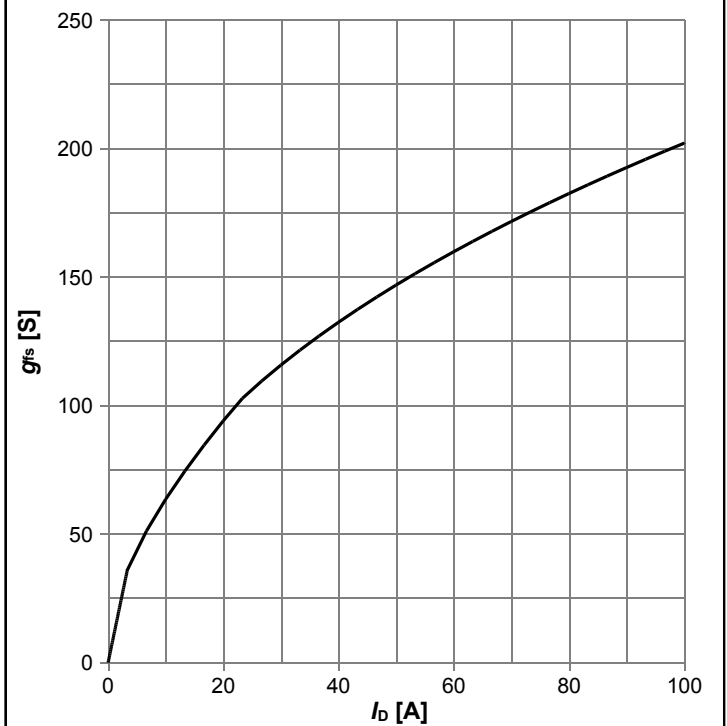
$R_{DS(on)} = f(I_D)$ ;  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



$I_D = f(V_{GS})$ ;  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

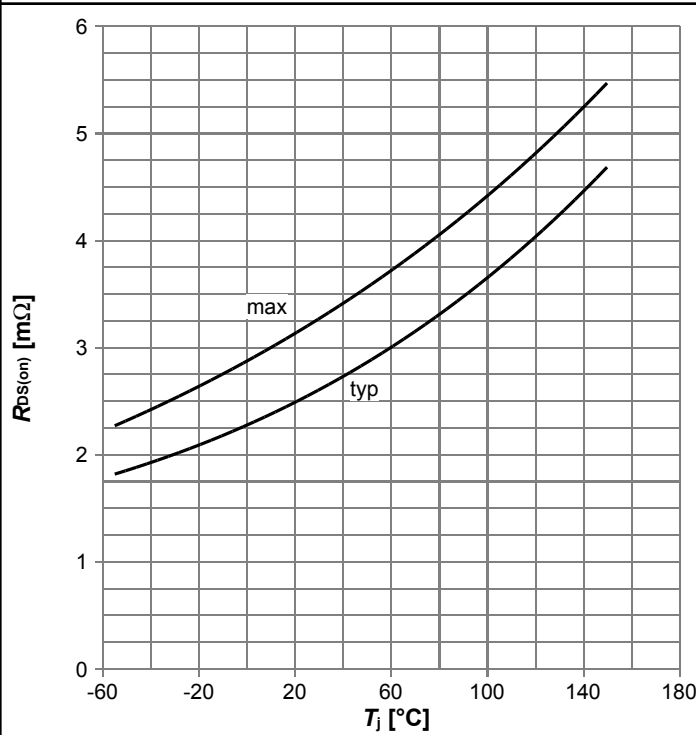
Diagram 8: Typ. forward transconductance



$g_{fs} = f(I_D)$ ;  $T_j = 25\text{ °C}$

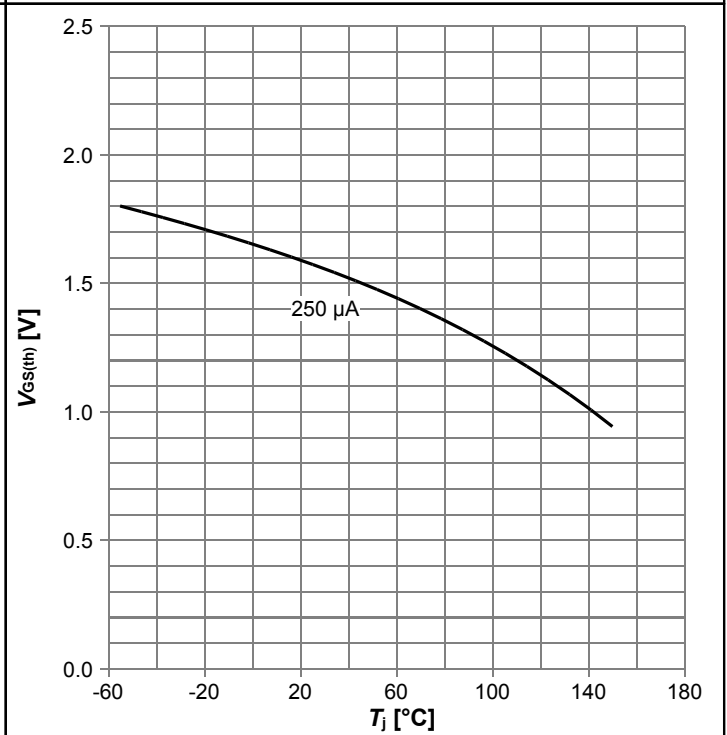


Diagram 9: Drain-source on-state resistance



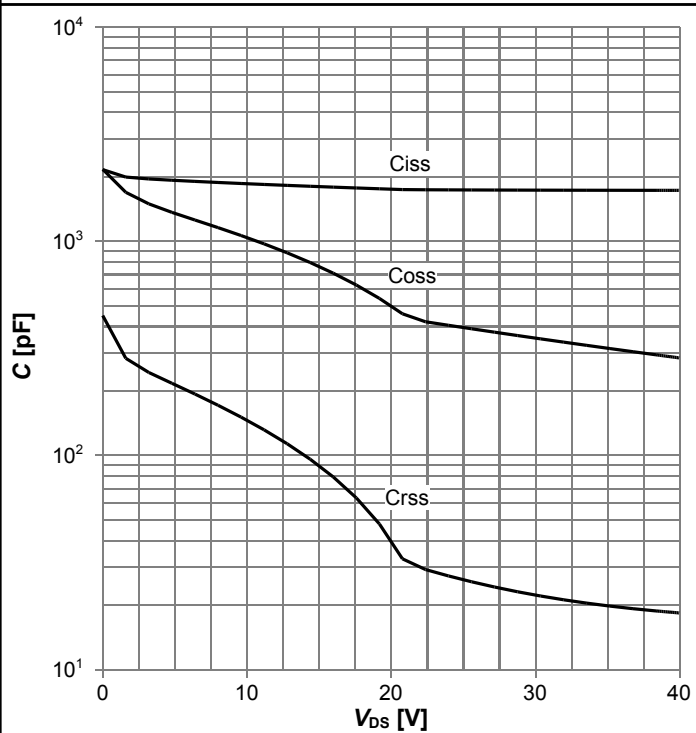
$R_{DS(on)}=f(T_j)$ ;  $I_D=50$  A;  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



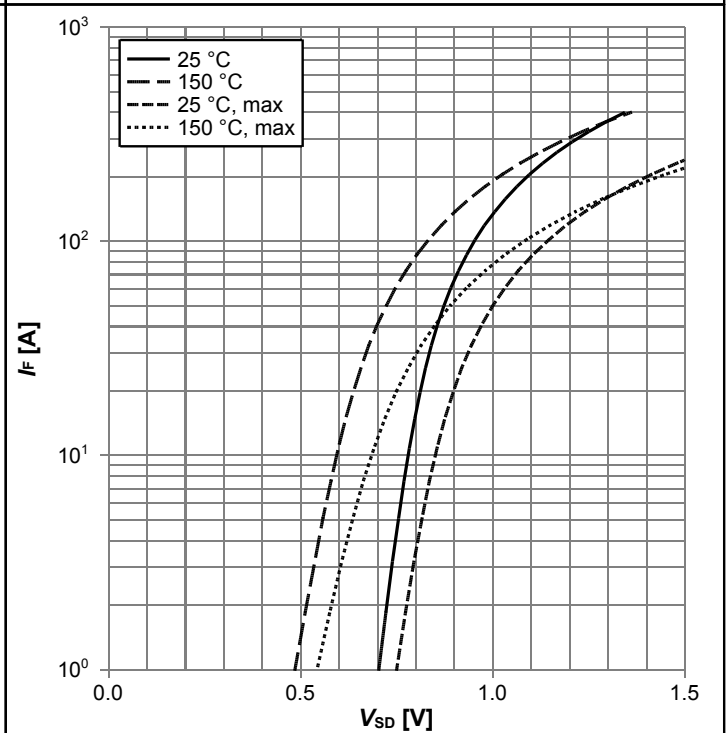
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ;  $I_D=250$   $\mu$ A

Diagram 11: Typ. capacitances



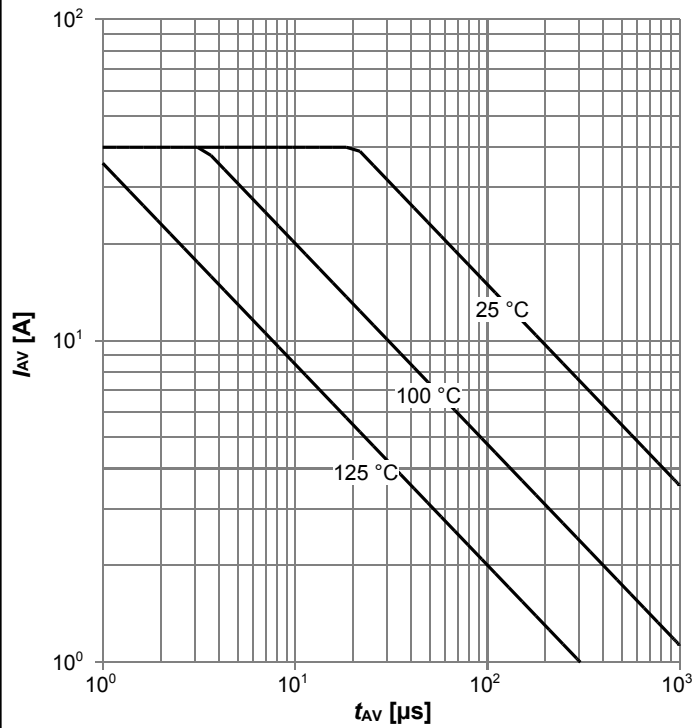
$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

Diagram 12: Forward characteristics of reverse diode



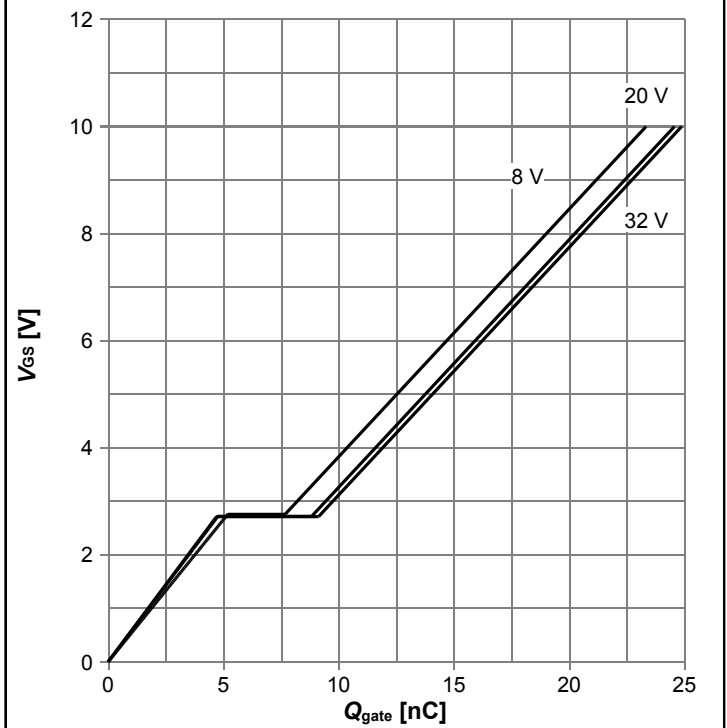
$I_F=f(V_{SD})$ ; parameter:  $T_j$

Diagram 13: Avalanche characteristics



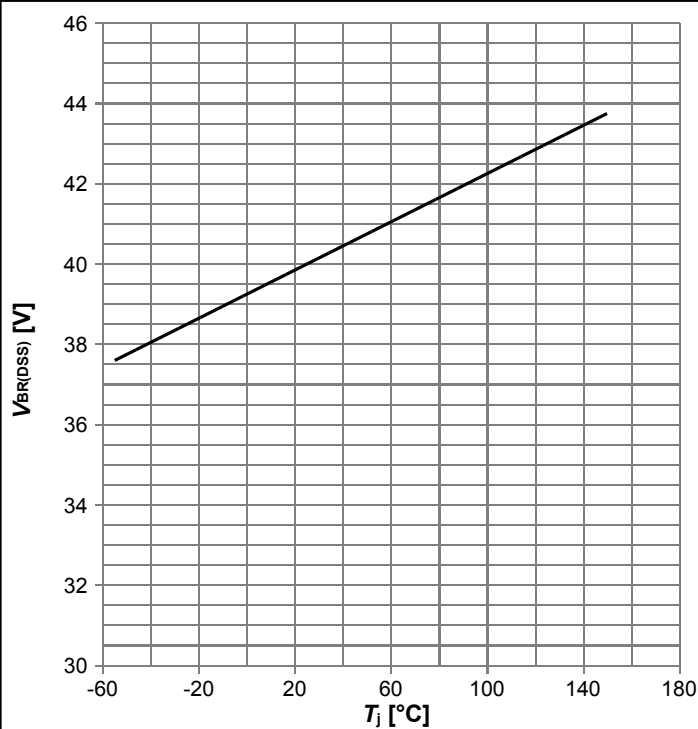
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



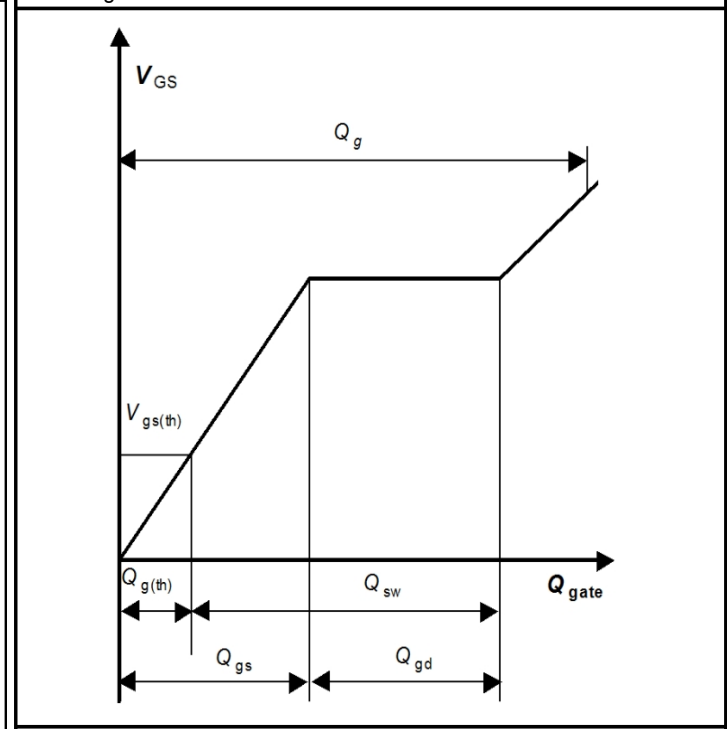
$V_{GS}=f(Q_{gate}); I_D=50 \text{ A}$  pulsed; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage

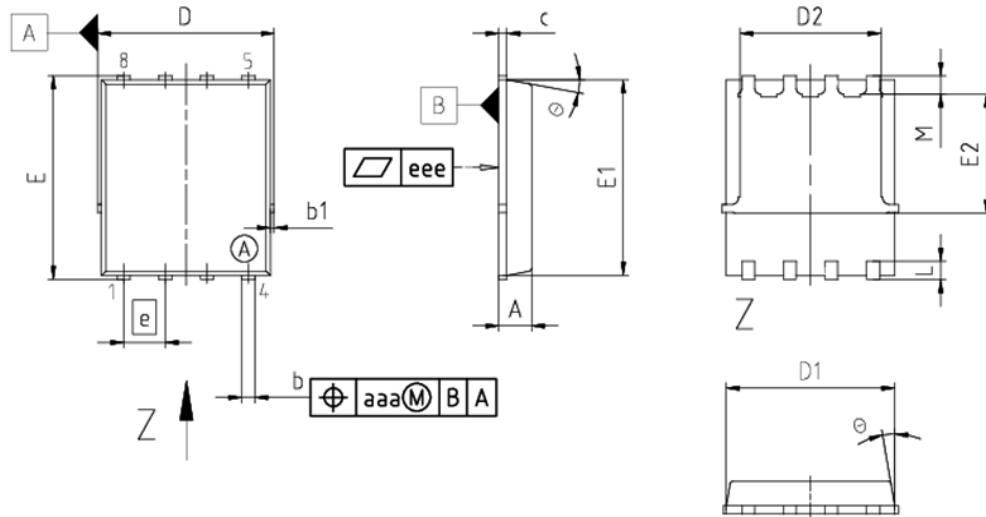


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



### 5 Package Outlines



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
theta	8.5°	12°
aaa	0.25	
eee	0.08	

**DOCUMENT NO.**  
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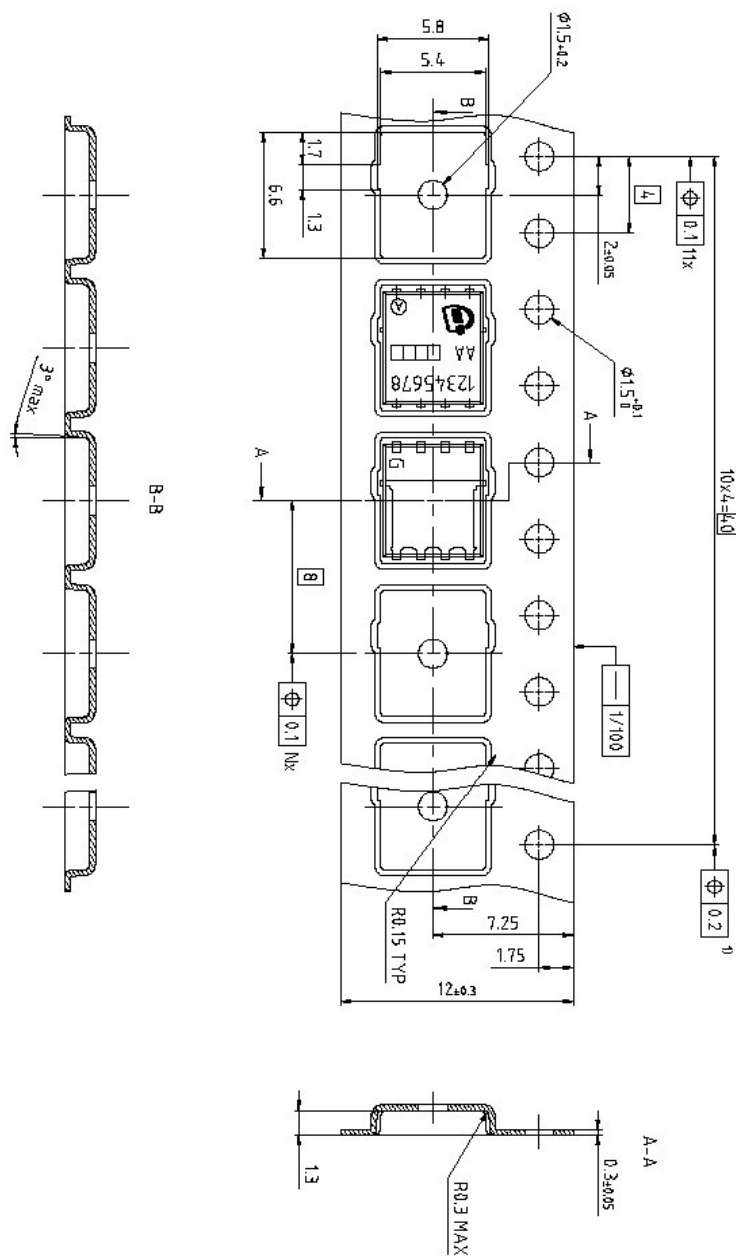
**SCALE**  
0 2 4mm

**EUROPEAN PROJECTION**

**ISSUE DATE**  
10-04-2013

**REVISION**  
04

Figure 1 Outline PG-TDSON-8, dimensions in mm



Dimension in mm

Figure 2 Outline Tape (TDSON-8)

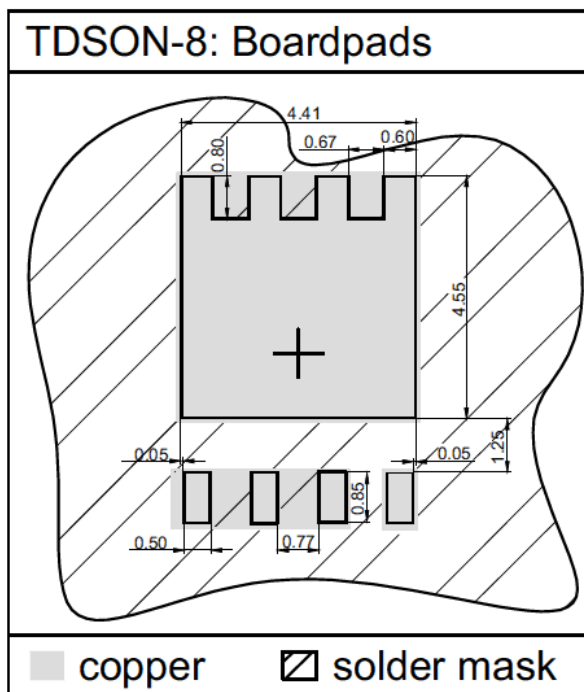


Figure 3 Outline Footprint (TDSO-8)

## Revision History

BSC032N04LS

**Revision: 2016-06-09, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2016-06-09	Insert max values and update footnotes

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**Infineon Technologies AG**  
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