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ADS7951QDBTRQ1

Texas instruments

Analog to Digital Converters - ADC Auto 12bit, 1 MSPS 8Ch Sng-end, SAR ADC

Any questions,please feel free to contact us.
info@kaimte.com

TEXAS INSTRUMENTS

ADS7950-Q1, ADS7951-Q1, ADS7952-Q1, ADS7953-Q1, ADS7954-Q1
ADS7956-Q1, ADS7957-Q1, ADS7958-Q1, ADS7959-Q1, ADS7960-Q1, ADS7961-Q1

SBAS652A – MAY 2014 – REVISED AUGUST 2014

ADS79xx-Q1 8-, 10-, and 12-Bit, 1-MSPS, 4-, 8-, 12-, and 16-Channel, Single-Ended, Micropower, Serial Interface, Analog-to-Digital Converters

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Tested with the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Product Family:
  - 8-, 10-, and 12-Bit Resolution
  - 4-, 8-, 12-Channel Devices Share 16-Channel Footprint
- 1-MHz Sample-Rate Serial Devices
- Analog Supply Range: 2.7 V to 5.25 V
- I/O Supply Range: 1.7 V to 5.25 V
- Two SW-Selectable Unipolar, Input Ranges:
  - (0 V to 2.5 V) or (0 V to 5 V)
- Auto and Manual Modes for Channel Selection
- Two Programmable Alarm Levels per Channel
- Four Individually Configurable GPIOs
- Typical Power Dissipation: 14.5 mW ($V_{(+VA)}$ = 5 V, $V_{(+VBD)}$ = 3 V) at 1 MSPS
- Power-Down Current (1 µA)
- 30-Pin and 38-Pin TSSOP Package

2 Applications

- Automotive Systems
- Power Supply Monitoring
- Battery-Powered Systems
- High-Speed, Data-Acquisition Systems

3 Description

The ADS79xx-Q1 device family consists of multichannel 8-bit, 10-bit and 12-bit analog-to-digital converters (ADCs). The devices include a capacitor-based successive approximation register (SAR) ADC with inherent sample and hold. Multiple features and great performance makes the ADS79xx-Q1 device useful for wide variety of applications where multiple channels should be monitored.

The ADS79xx-Q1 device works on a wide analog-supply range from 2.7 V to 5.25 V. These devices are suitable for battery-powered and isolated power-supply applications because of very-low power consumption.

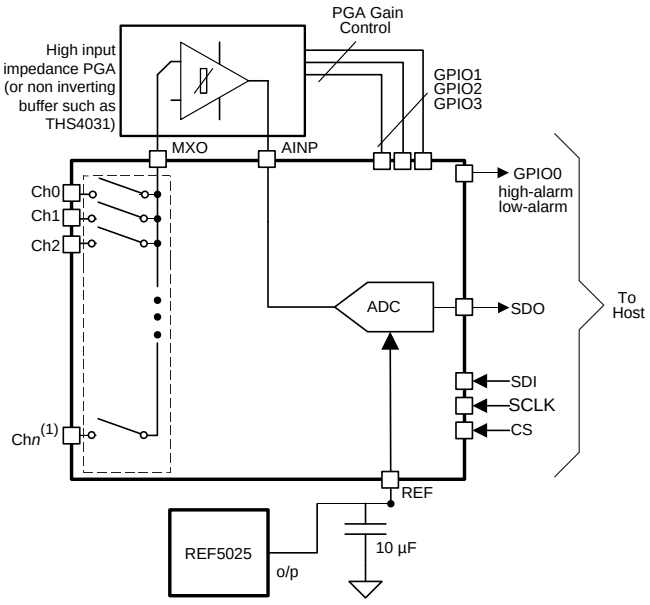
The 4- and 8-channel devices are available in 30-pin TSSOP package. The 12- and 16-channel devices are available in 38-pin TSSOP package.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE
ADS7950-Q1	TSSOP (30)	7.80 mm × 4.40 mm
ADS7951-Q1		
ADS7954-Q1		
ADS7958-Q1		
ADS7959-Q1		
ADS7952-Q1	TSSOP (38)	9.70 mm × 4.40 mm
ADS7953-Q1		
ADS7956-Q1		
ADS7957-Q1		
ADS7960-Q1		
ADS7961-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Detailed Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (May 2014) to Revision A **Page**

- Added all devices to Device Information table ... 1
- Deleted Device Comparison Table footnote ... 3
- Changed entire *Application and Implementation* section ... 40

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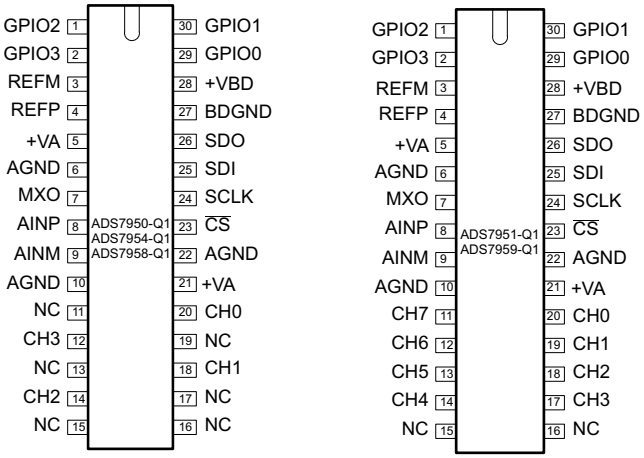
5 Device Comparison Table

NUMBER OF CHANNELS	RESOLUTION		
	12 BIT	10 BIT	8 BIT
4	ADS7950-Q1	ADS7954-Q1	ADS7958-Q1
8	ADS7951-Q1	—	ADS7959-Q1
12	ADS7952-Q1	ADS7956-Q1	ADS7960-Q1
16	ADS7953-Q1	ADS7957-Q1	ADS7961-Q1

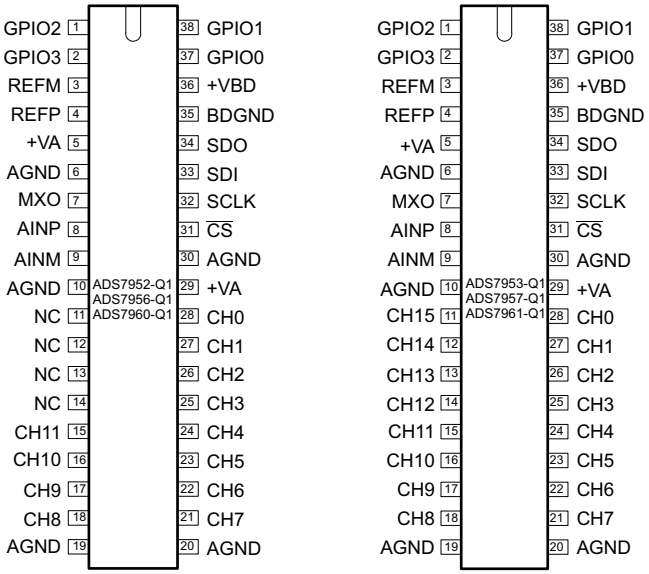
6 Pin Configurations and Functions

DBT Package
TSSOP-30
(Top View)



NC = No internal connection

DBT Package
TSSOP-38
(Top View)



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Pin Functions

PIN					I/O	DESCRIPTION
NAME	NUMBER					
	ADS7953-Q1, ADS7957-Q1, ADS7961-Q1	ADS7952-Q1, ADS7956-Q1, ADS7960-Q1	ADS7951-Q1, ADS7959-Q1	ADS7950-Q1, ADS7954-Q1, ADS7958-Q1		
ADC ANALOG INPUT						
AINM	9	9	9	9	I	ADC input ground
AINP	8	8	8	8	I	Signal input to ADC
DIGITAL CONTROL SIGNALS						
$\overline{CS}$	31	31	23	23	I	Chip-select input
SCLK	32	32	24	24	I	Serial clock input
SDI	33	33	25	25	I	Serial data input
SDO	34	34	26	26	O	Serial data output
GENERAL PURPOSE INPUTS AND OUTPUTS(1)						
GPIO0	37	37	29	29	I/O	General-purpose input or output
High or low alarm					O	Active high output indicating high alarm or low alarm, depending on programming
GPIO1	38	38	30	30	I/O	General-purpose input or output
Low alarm					O	Active high output indicating low alarm
GPIO2	1	1	1	1	I/O	General-purpose input or output
Range					I	Selects range: High → Range 2; Low → Range 1
GPIO3	2	2	2	2	I/O	Genera-purpose input or output
$\overline{PD}$					I	Active low power-down input
MULTIPLEXER						
Ch0	28	28	20	20	I	Analog channels for multiplexer
Ch1	27	27	19	18	I	
Ch2	26	26	18	14	I	
Ch3	25	25	17	12	I	
Ch4	24	24	14	—	I	
Ch5	23	23	13	—	I	
Ch6	22	22	12	—	I	
Ch7	21	21	11	—	I	
Ch8	18	18	—	—	I	
Ch9	17	17	—	—	I	
Ch10	16	16	—	—	I	
Ch11	15	15	—	—	I	
Ch12	14	—	—	—	I	
Ch13	13	—	—	—	I	
Ch14	12	—	—	—	I	
Ch15	11	—	—	—	I	
MXO	7	7	7	7	O	Multiplexer output
NC PINS						
NC	—	11	15	11	—	Pins internally not connected, do not float these pins
		12	16	13		
		13	—	15		
		14	—	16		
		—	—	17		
		—	—	19		

(1) These pins have programmable dual functionality. See Table 12 for functionality programming.

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Pin Functions (continued)

PIN					I/O	DESCRIPTION
NAME	NUMBER					
	ADS7953-Q1, ADS7957-Q1, ADS7961-Q1	ADS7952-Q1, ADS7956-Q1, ADS7960-Q1	ADS7951-Q1, ADS7959-Q1	ADS7950-Q1, ADS7954-Q1, ADS7958-Q1		
POWER SUPPLY AND GROUND						
AGND	6	6	6	6	—	Analog ground
	10	10	10	10		
	19	19	22	22		
	20	20	—	—		
	30	30	—	—		
BDGND	35	35	27	27	—	Digital ground
+VA	5	5	5	5	—	Analog power supply
	29	29	21	21		
+VBD	36	36	28	28	—	Digital I/O supply
REFERENCE						
REFM	3	3	3	3	I	Reference ground
REFP	4	4	4	4	I	Reference input

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
Supply voltage to ground	+VA to AGND, +VBD to BDGND	–0.3	7	V
Signal input	AINP or CHn to AGND	–0.3	$V_{(+VA)}$ + 0.3	V
Digital input	To BDGND	–0.3	7	V
Digital output	To BDGND	–0.3	$V_{(+VA)}$ + 0.3	V
Junction temperature, T_J			150	°C

(1) Stresses beyond those listed as *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated as *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), level H2		–2	2	kV
		Charged-device model (CDM), per AEC Q100-001, level C4B	Corner pins (1, 15, 16, and 30 for 30-pin packages 1, 19, 20, and 38 for 38-pin packages)	–750	750	V
			All pins	–500	500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{(+VA)}$	Analog power-supply voltage	2.7	3.3	5.25	V
$V_{(+VBD)}$	Digital I/O-supply voltage	1.7	3.3	$V_{(+VA)}$	V
$V_{(REF)}$	Reference voltage	2	2.5	3	V
$f_{(SCLK)}$	SCLK frequency			20	MHz
T_A	Operating temperature range	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		ADS79xx-Q1		UNIT
		DBT (TSSOP)	DBT (TSSOP)	
		38 PINS	30 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.6	89.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.8	22.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.7	43.1	
ψ_{JT}	Junction-to-top characterization parameter	2.9	0.8	
ψ_{JB}	Junction-to-board characterization parameter	44.1	42.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: ADS7950-Q1, ADS7951-Q1, ADS7952-Q1, ADS7953-Q1

$V_{(+VA)}$ = 2.7 V to 5.25 V, $V_{(+VBD)}$ = 1.7 V to $V_{(+VA)}$, V_{ref} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input span(1)	Range 1	0		V_{ref}	V
		Range 2 while 2 × V_{ref} ≤ +VA	0		2 × V_{ref}	V
	Absolute input range	Range 1	–0.2		V_{ref} + 0.2	V
		Range 2 while 2 × V_{ref} ≤ +VA	–0.2		2 × V_{ref} + 0.2	V
	Input capacitance			15		ρF
	Input leakage current	T_A = 125°C		61		nA
SYSTEM PERFORMANCE						
	Resolution			12		Bits
	No missing codes		11			Bits
	Integral linearity		–1.5	±0.75	1.5	LSB(2)
	Differential linearity		–2	±0.75	1.5	LSB
	Offset error(3)		–3.5	±1.1	3.5	LSB
	Gain error	Range 1	–2	±0.2	2	LSB
		Range 2		±0.2		LSB
TUE	Total unadjusted error			±2		LSB
SAMPLING DYNAMICS						
	Conversion time	20-MHz SCLK			800	ns
	Acquisition time		325			ns
	Maximum throughput rate	20-MHz SCLK			1	MHz
	Aperture delay			5		ns
	Step response			150		ns
	Over voltage recovery			150		ns

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least-significant bit.
(3) Measured relative to an ideal full-scale input

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Electrical Characteristics: ADS7950-Q1, ADS7951-Q1, ADS7952-Q1, ADS7953-Q1 (continued)

$V_{(+VA)}$ = 2.7 V to 5.25 V, $V_{(+VBD)}$ = 1.7 V to $V_{(+VA)}$, V_{ref} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS						
THD	Total harmonic distortion(4)	100 kHz		–82		dB
SNR	Signal-to-noise ratio	100 kHz	70	71.7		dB
SINAD	Signal-to-noise + distortion	100 kHz	68	71.3		dB
SFDR	Spurious-free dynamic range	100 kHz		84		dB
	Small signal bandwidth	At –3 dB		47		MHz
	Channel-to-channel crosstalk	Any off-channel with 100 kHz. Full-scale input to channel being sampled with DC input (isolation crosstalk).		–95		dB
		From previously sampled to channel with 100 kHz. Full-scale input to channel being sampled with DC input (memory crosstalk).		–85		dB
EXTERNAL REFERENCE INPUT						
V_{ref}	Reference voltage at REFP(5)		2	2.5	3	V
R_{ref}	Reference resistance			100		kΩ
ALARM SETTING						
	Higher threshold range		0		FFC	Hex
	Lower threshold range		0		FFC	Hex
DIGITAL INPUT/OUTPUT (CMOS Logic Family)						
V_{IH}	High logic-level input voltage		0.7 × $V_{(+VBD)}$			V
V_{IL}	Low logic-level input voltage	$V_{(+VA)}$ = 5 V			0.8	V
		$V_{(+VA)}$ = 3 V			0.4	V
V_{OH}	High logic-level output voltage	At source current (I_S) = 200 µA	$V_{(+VBD)}$ – 0.2			V
V_{OL}	Low logic-level output voltage	At I_{sink} = 200 µA			0.4	V
	Data format MSB first			MSB first		
POWER SUPPLY REQUIREMENTS						
$V_{(+VA)}$	Analog power-supply voltage		2.7	3.3	5.25	V
$V_{(+VBD)}$	Digital I/O-supply voltage		1.7	3.3	$V_{(+VA)}$	V
$I_{(+VA)}$	Supply current (normal mode)	At $V_{(+VA)}$ = 2.7 V to 3.6 V and 1-MHz throughput		1.8		mA
		At $V_{(+VA)}$ = 2.7 V to 3.6 V static state		1.05		mA
		At $V_{(+VA)}$ = 4.7 V to 5.25 V and 1-MHz throughput		2.3	3	mA
		At $V_{(+VA)}$ = 4.7 V to 5.25 V static state		1.1	1.5	mA
	Power-down state supply current			1		µA
$I_{(+VBD)}$	Digital I/O-supply current	$V_{(+VA)}$ = 5.25 V, f_{sample} = 1 MHz		1		mA
	Power-up time				1	µs
	Invalid conversions after power up or reset				1	cycle
	Latch-up			JESD78 class I		
TEMPERATURE RANGE						
	Specified performance		–40		125	°C

(4) Calculated on the first nine harmonics of the input frequency.
(5) The device is designed to operate over V_{ref} = 2 V to 3 V. However, lower noise performance can be expected at V_{ref} < 2.4 V, because of SNR degradation resulting from lowered signal range.

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7.6 Electrical Characteristics: ADS7954-Q1, ADS7956-Q1, ADS7957-Q1

$V_{(+VA)}$ = 2.7 V to 5.25 V, $V_{(+VBD)}$ = 1.7 V to $V_{(+VA)}$, V_{ref} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input span(1)	Range 1	0		V_{ref}	V
		Range 2 while 2 × V_{ref} ≤ +VA	0		2 × V_{ref}	V
	Absolute input range	Range 1	–0.2		V_{ref} + 0.2	V
		Range 2 while 2 × V_{ref} ≤ +VA	–0.2		2 × V_{ref} +0.2	V
	Input capacitance			15		pF
	Input leakage current	T_A = 125°C		61		nA
SYSTEM PERFORMANCE						
	Resolution			10		Bits
	No missing codes		10			Bits
	Integral linearity		–0.5	±0.2	0.5	LSB(2)
	Differential linearity		–0.5	±0.2	0.5	LSB
	Offset error(3)		–1.5	±0.5	1.5	LSB
	Gain error	Range 1	–1	±0.1	1	LSB
		Range 2		±0.1		LSB
SAMPLING DYNAMICS						
	Conversion time	20-MHz SCLK			800	ns
	Acquisition time		325			ns
	Maximum throughput rate	20-MHz SCLK			1	MHz
	Aperture delay			5		ns
	Step response			150		ns
	Over voltage recovery			150		ns
DYNAMIC CHARACTERISTICS						
THD	Total harmonic distortion(4)	100 kHz		–80		dB
SNR	Signal-to-noise ratio	100 kHz	60			dB
SINAD	Signal-to-noise + distortion	100 kHz	60			dB
SFDR	Spurious-free dynamic range	100 kHz		82		dB
	Full-power bandwidth	At –3 dB		47		MHz
	Channel-to-channel crosstalk	Any off-channel with 100 kHz. Full-scale input to channel being sampled with dc input.		–95		dB
		From previously sampled to channel with 100 kHz. Full-scale input to channel being sampled with dc input.		–85		dB
EXTERNAL REFERENCE INPUT						
V_{ref}	Reference voltage at REFP		2	2.5	3	V
R_{ref}	Reference resistance			100		kΩ
ALARM SETTING						
	Higher threshold range		000		FFC	Hex
	Lower threshold range		000		FFC	Hex
DIGITAL INPUT/OUTPUT (CMOS Logic Family)						
V_{IH}	High logic-level input voltage		0.7 × $V_{(+VBD)}$			V
V_{IL}	Low logic-level input voltage	$V_{(+VBD)}$ = 5 V			0.8	V
		$V_{(+VBD)}$ = 3 V			0.4	V
V_{OH}	High logic-level output voltage	At source current (I_S) = 200 µA	$V_{(+VBD)}$ – 0.2			V
V_{OL}	Low logic-level output voltage	At I_{sink} = 200 µA	0.4			V
	Data format MSB first			MSB first		

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input
(4) Calculated on the first nine harmonics of the input frequency.

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Electrical Characteristics: ADS7954-Q1, ADS7956-Q1, ADS7957-Q1 (continued)

$V_{(+VA)}$ = 2.7 V to 5.25 V, $V_{(+VBD)}$ = 1.7 V to $V_{(+VA)}$, V_{ref} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY REQUIREMENTS						
$V_{(+VA)}$	Analog power-supply voltage		2.7	3.3	5.25	V
$V_{(+VBD)}$	Digital I/O-supply voltage		1.7	3.3	$V_{(+VA)}$	V
$I_{(+VA)}$	Supply current (normal mode)	At $V_{(+VA)}$ = 2.7 V to 3.6 V and 1-MHz throughput		1.8		mA
		At $V_{(+VA)}$ = 2.7 V to 3.6 V static state		1.05	1	mA
		At $V_{(+VA)}$ = 4.7 V to 5.25 V and 1-MHz throughput		2.3	3	mA
		At $V_{(+VA)}$ = 4.7 V to 5.25 V static state		1.1	1.5	mA
	Power-down state supply current			1		µA
$I_{(+VBD)}$	Digital I/O-supply current	$V_{(+VA)}$ = 5.25 V, f_{sample} = 1 MHz		1		mA
	Power-up time				1	µs
	Invalid conversions after power up or reset				1	cycle
	Latch-up			JESD78 class I		
TEMPERATURE RANGE						
	Specified performance		–40		125	°C

7.7 Electrical Characteristics: ADS7958-Q1, ADS7959-Q1, ADS7960-Q1, ADS7961-Q1

$V_{(+VA)}$ = 2.7 V to 5.25 V, $V_{(+VBD)}$ = 1.7 V to $V_{(+VA)}$, V_{ref} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input span(1)	Range 1	0		V_{ref}	V
		Range 2 while 2 × V_{ref} ≤ +VA	0		2 × V_{ref}	V
	Absolute input range	Range 1	–0.20		V_{ref} + 0.2	V
		Range 2 while 2 × V_{ref} ≤ +VA	–0.20		2 × V_{ref} + 0.2	V
	Input capacitance			15		pF
	Input leakage current	T_A = 125°C		61		nA
SYSTEM PERFORMANCE						
	Resolution			8		Bits
	No missing codes		8			Bits
	Integral linearity		–0.3	±0.1	0.3	LSB(2)
	Differential linearity		–0.3	±0.1	0.3	LSB
	Offset error(3)		–0.5	±0.2	0.5	LSB
	Gain error	Range 1	–0.6	±0.1	0.6	LSB
		Range 2		±0.1		LSB
SAMPLING DYNAMICS						
	Conversion time	20-MHz SCLK			800	ns
	Acquisition time		325			ns
	Maximum throughput rate	20-MHz SCLK			1	MHz
	Aperture delay			5		ns
	Step response			150		ns
	Over voltage recovery			150		ns

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input

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Electrical Characteristics: ADS7958-Q1, ADS7959-Q1, ADS7960-Q1, ADS7961-Q1 (continued)

$V_{(+VA)}$ = 2.7 V to 5.25 V, $V_{(+VBD)}$ = 1.7 V to $V_{(+VA)}$, V_{ref} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS						
THD	Total harmonic distortion(4)	100 kHz		–75		dB
SNR	Signal-to-noise ratio	100 kHz	49			dB
SINAD	Signal-to-noise + distortion	100 kHz	49			dB
SFDR	Spurious-free dynamic range	100 kHz		–78		dB
	Full-power bandwidth	At –3 dB		47		MHz
	Channel-to-channel crosstalk	Any off-channel with 100 kHz. Full-scale input to channel being sampled with dc input.		–95		dB
		From previously sampled to channel with 100 kHz. Full-scale input to channel being sampled with dc input.		–85		dB
EXTERNAL REFERENCE INPUT						
Vref	reference voltage at REFP		2	2.5	3	V
	Reference resistance			100		kΩ
ALARM SETTING						
	Higher threshold range		000		FF	Hex
	Lower threshold range		000		FF	Hex
DIGITAL INPUT/OUTPUT (CMOS Logic Family)						
V_{IH}	High logic-level input voltage		0.7 × $V_{(+VBD)}$			V
V_{IL}	Low logic-level input voltage	$V_{(+VBD)}$ = 5 V			0.8	V
		$V_{(+VBD)}$ = 3 V			0.4	V
V_{OH}	High logic-level output voltage	At source current (I_S) = 200 µA	$V_{(+VBD)}$ – 0.2			V
V_{OL}	Low logic-level output voltage	At I_{sink} = 200 µA		0.4		V
	Data format			MSB first		
POWER SUPPLY REQUIREMENTS						
$V_{(+VA)}$	Analog power-supply voltage		2.7	3.3	5.25	V
$V_{(+VBD)}$	Digital I/O-supply voltage		1.7	3.3	$V_{(+VA)}$	V
$I_{(+VA)}$	Supply current (normal mode)	At $V_{(+VA)}$ = 2.7 V to 3.6 V and 1-MHz throughput		1.8		mA
		At $V_{(+VA)}$ = 2.7 V to 3.6 V static state		1.05		mA
		At $V_{(+VA)}$ = 4.7 V to 5.25 V and 1-MHz throughput		2.3	3	mA
		At $V_{(+VA)}$ = 4.7 V to 5.25 V static state		1.1	1.5	mA
	Power-down state supply current			1		µA
$I_{(+VBD)}$	Digital I/O-supply current	$V_{(+VA)}$ = 5.25 V, f_{sample} = 1 MHz		1		mA
	Power-up time				1	µs
	Invalid conversions after power up or reset				1	cycle
	Latch-up			JESD78 class I		
TEMPERATURE RANGE						
	Specified performance		–40		125	°C

(4) Calculated on the first nine harmonics of the input frequency.

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7.8 Timing Requirements

All specifications typical at –40°C to 125°C, $V_{(+VA)}$ = 2.7 V to 5.25 V (unless otherwise specified). See Figure 45, Figure 46, Figure 47, and Figure 48.

PARAMETER[1][2]			MIN	TYP	MAX	UNIT
t_c	Conversion time	$V_{(+VBD)}$ = 1.8 V			16	SCLK
		$V_{(+VBD)}$ = 3 V			16	SCLK
		$V_{(+VBD)}$ = 5 V			16	SCLK
t_q	Minimum quiet sampling time needed from bus Tri-state to start of next conversion	$V_{(+VBD)}$ = 1.8 V	40			ns
		$V_{(+VBD)}$ = 3 V	40			ns
		$V_{(+VBD)}$ = 5 V	40			ns
t_{d1}	Delay time, $\overline{CS}$ low to first data (DO–15) out	$V_{(+VBD)}$ = 1.8 V			38	ns
		$V_{(+VBD)}$ = 3 V			27	ns
		$V_{(+VBD)}$ = 5 V			17	ns
t_{su1}	Setup time, $\overline{CS}$ low to first rising edge of SCLK	$V_{(+VBD)}$ = 1.8 V	8			ns
		$V_{(+VBD)}$ = 3 V	6			ns
		$V_{(+VBD)}$ = 5 V	4			ns
t_{d2}	Delay time, SCLK falling to SDO next data bit valid	$V_{(+VBD)}$ = 1.8 V			35	ns
		$V_{(+VBD)}$ = 3 V			27	ns
		$V_{(+VBD)}$ = 5 V			17	ns
t_{h1}	Hold time, SCLK falling to SDO data bit valid	$V_{(+VBD)}$ = 1.8 V	7			ns
		$V_{(+VBD)}$ = 3 V	5			ns
		$V_{(+VBD)}$ = 5 V	3			ns
t_{d3}	Delay time, 16th SCLK falling edge to SDO 3-state	$V_{(+VBD)}$ = 1.8 V			26	ns
		$V_{(+VBD)}$ = 3 V			22	ns
		$V_{(+VBD)}$ = 5 V			13	ns
t_{su2}	Setup time, SDI valid to rising edge of SCLK	$V_{(+VBD)}$ = 1.8 V	2			ns
		$V_{(+VBD)}$ = 3 V	3			ns
		$V_{(+VBD)}$ = 5 V	4			ns
t_{h2}	Hold time, rising edge of SCLK to SDI valid	$V_{(+VBD)}$ = 1.8 V	12			ns
		$V_{(+VBD)}$ = 3 V	10			ns
		$V_{(+VBD)}$ = 5 V	6			ns
t_{w1}	Pulse duration $\overline{CS}$ high	$V_{(+VBD)}$ = 1.8 V	20			ns
		$V_{(+VBD)}$ = 3 V	20			ns
		$V_{(+VBD)}$ = 5 V	20			ns
t_{d4}	Delay time $\overline{CS}$ high to SDO 3-state	$V_{(+VBD)}$ = 1.8 V			24	ns
		$V_{(+VBD)}$ = 3 V			21	ns
		$V_{(+VBD)}$ = 5 V			12	ns
t_{wH}	Pulse duration SCLK high	$V_{(+VBD)}$ = 1.8 V	20			ns
		$V_{(+VBD)}$ = 3 V	20			ns
		$V_{(+VBD)}$ = 5 V	20			ns
t_{wL}	Pulse duration SCLK low	$V_{(+VBD)}$ = 1.8 V	20			ns
		$V_{(+VBD)}$ = 3 V	20			ns
		$V_{(+VBD)}$ = 5 V	20			ns
$f_{(SCLK)}$	Frequency SCLK	$V_{(+VBD)}$ = 1.8 V			20	MHz
		$V_{(+VBD)}$ = 3 V			20	MHz
		$V_{(+VBD)}$ = 5 V			20	MHz

(1) 1.8-V specifications apply from 1.7 V to 1.9 V, 3-V specifications apply from 2.7 V to 3.6 V, 5-V specifications apply from 4.75 V to 5.25 V.
(2) With 50-pF load

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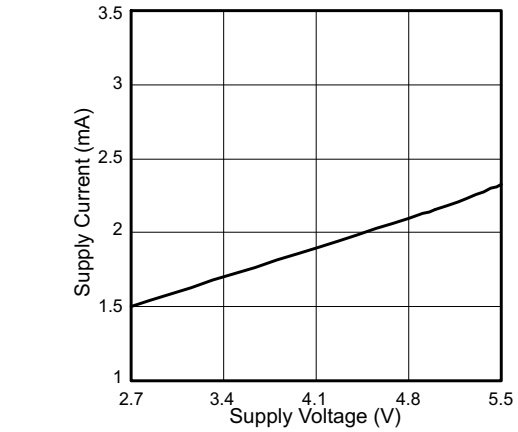
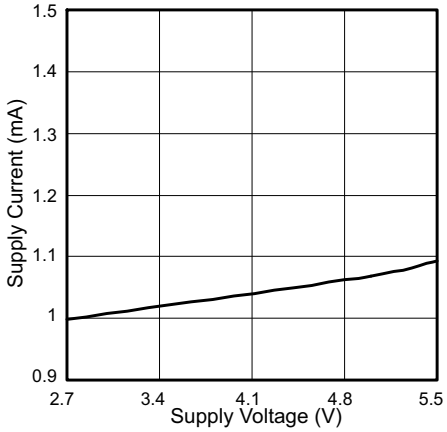
7.9 Typical Characteristics (All ADS79xx-Q1 Family Devices)



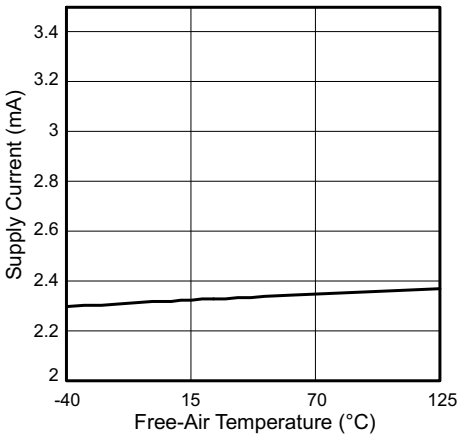
f_{sample} = 1 MSPS T_A = 25°C

Figure 1. Supply Current ($I_{(+VA)}$) vs Supply Voltage ($V_{(+VA)}$)



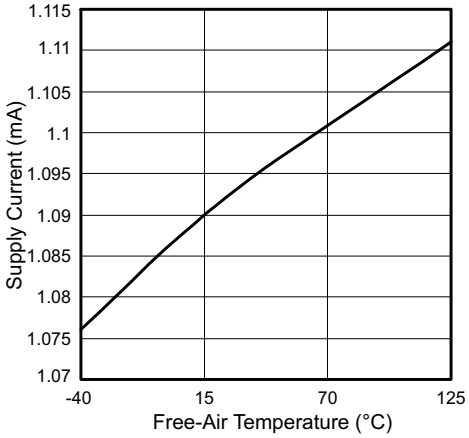
f_{sample} = 0 MSPS T_A = 25°C

Figure 2. Idle Supply Current ($I_{(+VA)}$) vs Supply Voltage ($V_{(+VA)}$)



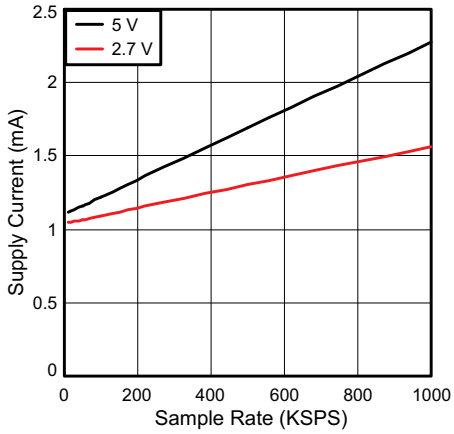
f_{sample} = 1 MSPS $V_{(+VBD)}$ = 5.5 V

Figure 3. Supply Current ($I_{(+VA)}$) vs Free-Air Temperature



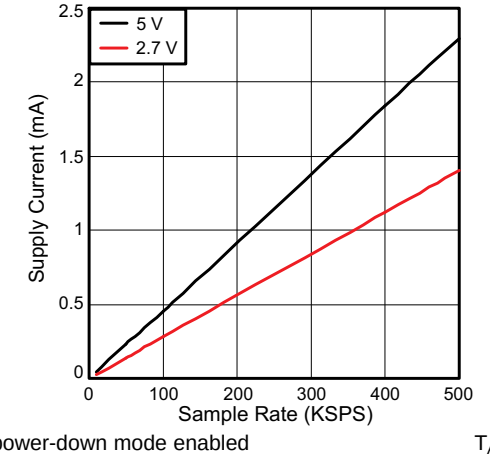
f_{sample} = 0 MSPS $V_{(+VBD)}$ = 5.5 V

Figure 4. Idle Supply Current ($I_{(+VA)}$) vs Free-Air Temperature



No power-down T_A = 25°C

Figure 5. Supply Current ($I_{(+VA)}$) vs Sample Rate



With power-down mode enabled T_A = 25°C

Figure 6. Supply Current ($I_{(+VA)}$) vs Sample Rate with Power-Down Mode Enabled

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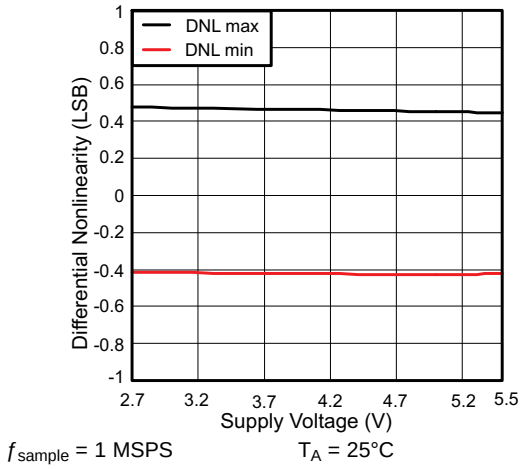
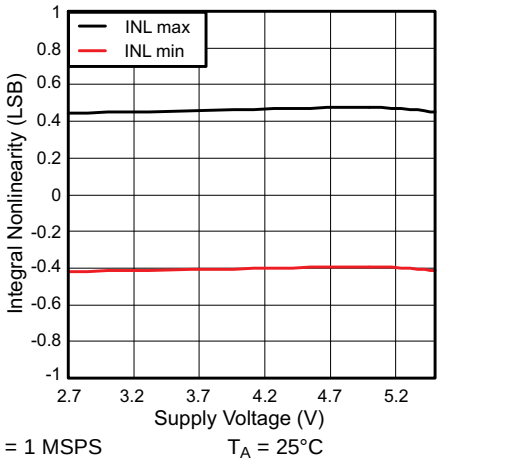
7.10 Typical Characteristics (12-Bit Devices Only)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves.



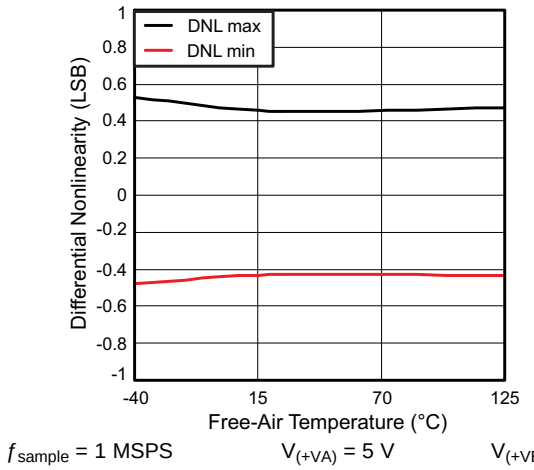
f_{sample} = 1 MSPS T_A = 25°C

Figure 7. Differential Nonlinearity vs Supply Voltage ($V_{(+VA)}$)



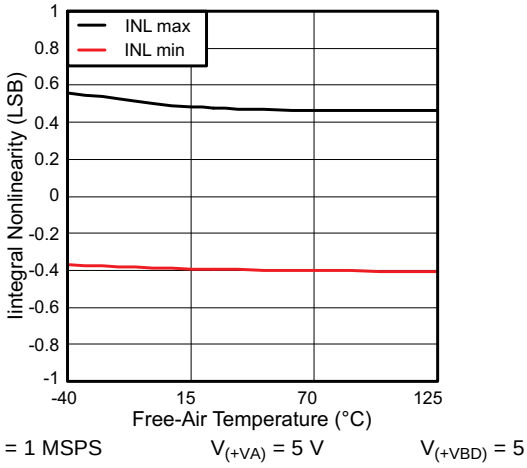
f_{sample} = 1 MSPS T_A = 25°C

Figure 8. Integral Nonlinearity vs Supply Voltage ($V_{(+VA)}$)



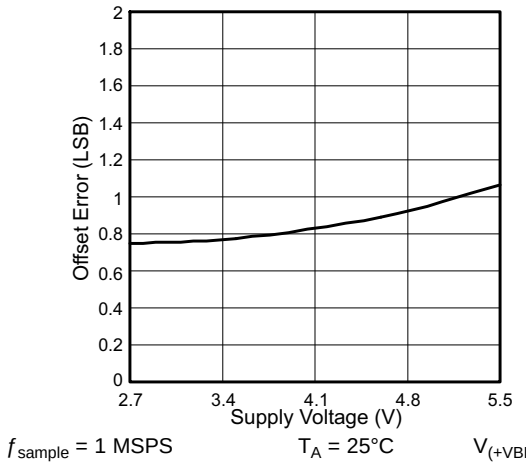
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V

Figure 9. Differential Nonlinearity vs Free-Air Temperature



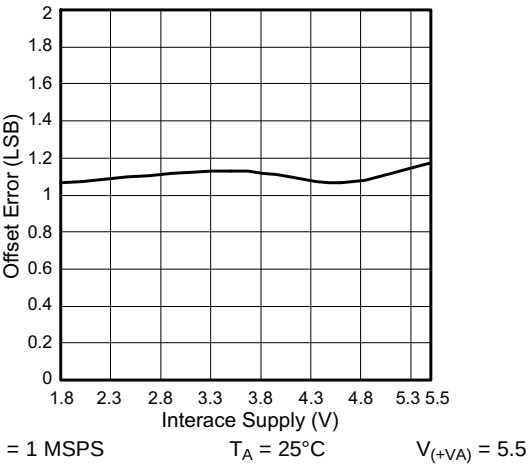
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V

Figure 10. Integral Nonlinearity vs Free-Air Temperature



f_{sample} = 1 MSPS T_A = 25°C $V_{(+VBD)}$ = 1.8 V

Figure 11. Offset Error vs Supply Voltage ($V_{(+VA)}$)

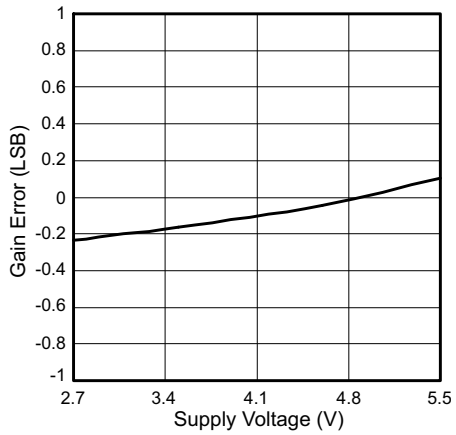


f_{sample} = 1 MSPS T_A = 25°C $V_{(+VA)}$ = 5.5 V

Figure 12. Offset Error vs Interface Supply Voltage ($V_{(+VBD)}$)

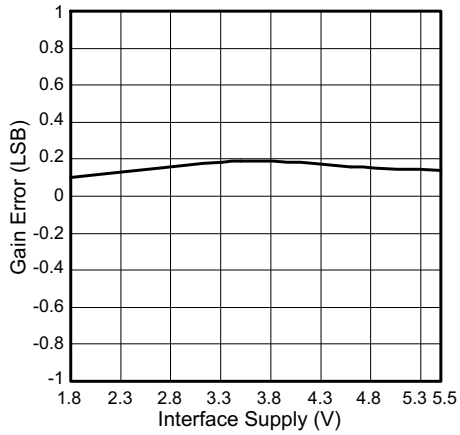
Typical Characteristics (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves.



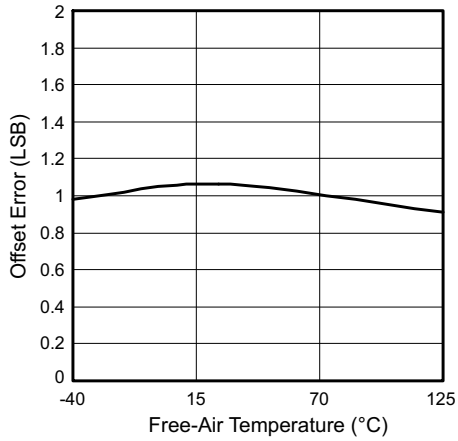
f_{sample} = 1 MSPS T_A = 25°C $V_{(+VBD)}$ = 1.8 V

Figure 13. Gain Error vs Supply Voltage ($V_{(+VA)}$)



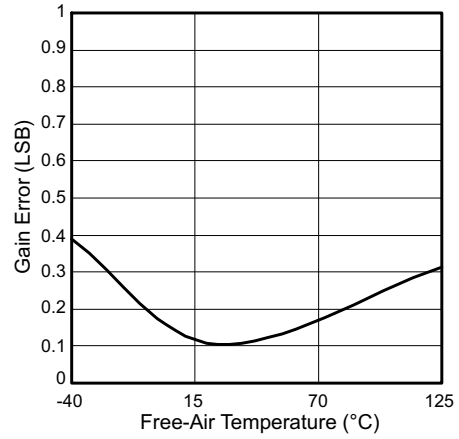
f_{sample} = 1 MSPS T_A = 25°C $V_{(+VA)}$ = 5.5 V

Figure 14. Gain Error vs Interface Supply Voltage ($V_{(+VBD)}$)



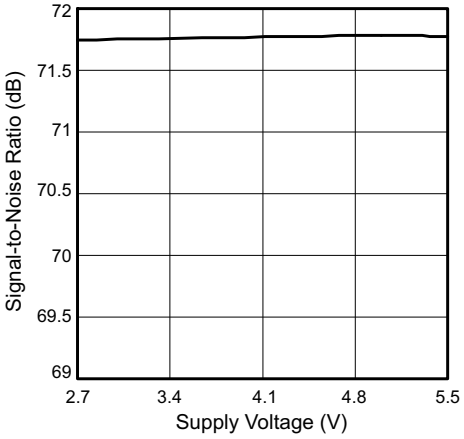
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5.5 V $V_{(+VBD)}$ = 1.8 V

Figure 15. Offset Error vs Free-Air Temperature



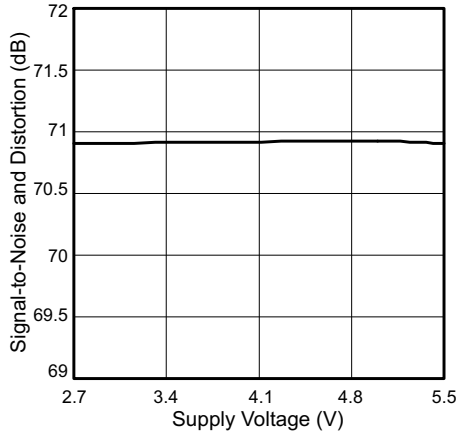
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5.5 V $V_{(+VBD)}$ = 1.8 V

Figure 16. Gain Error vs Free-Air Temperature



f_{sample} = 1 MSPS T_A = 25°C $V_{(+VBD)}$ = 3 V
f_{input} = 100 kHz

Figure 17. Signal-to-Noise Ratio vs Supply Voltage (+VA)



f_{sample} = 1 MSPS T_A = 25°C $V_{(+VBD)}$ = 3 V
f_{input} = 100 kHz

Figure 18. Signal-to-Noise With Distortion vs Supply Voltage ($V_{(+VA)}$)

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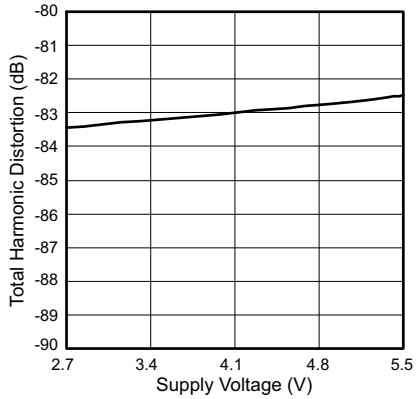
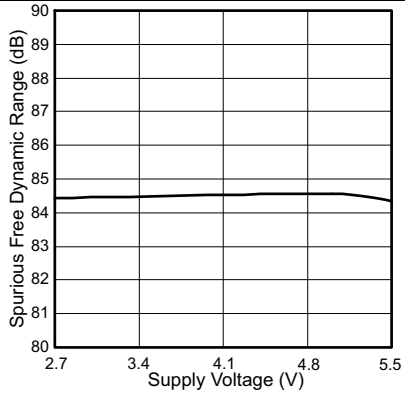
Typical Characteristics (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves.



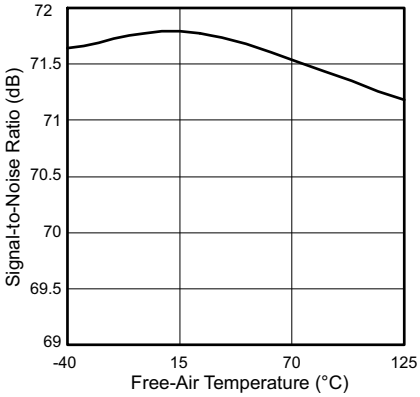
f_{sample} = 1 MSPS T_A = 25°C $V_{(+VBD)}$ = 3 V
f_{input} = 100 kHz

Figure 19. Total Harmonic Distortion (THD) vs Supply Voltage ($V_{(+VA)}$)



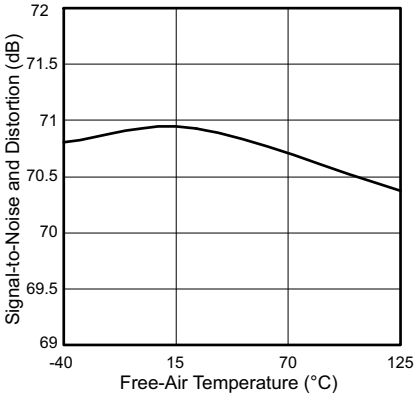
f_{sample} = 1 MSPS T_A = 25°C $V_{(+VBD)}$ = 3 V
f_{input} = 100 kHz

Figure 20. Spurious-Free Dynamic Range (SFDR) vs Supply Voltage ($V_{(+VA)}$)



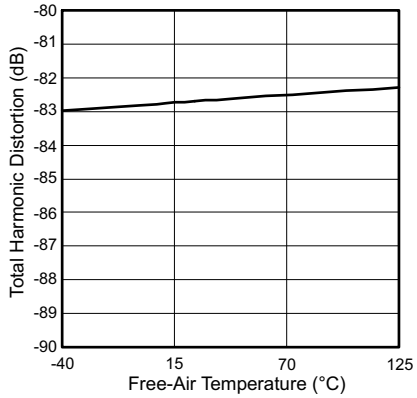
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 3 V
f_{input} = 100 kHz

Figure 21. Signal-to-Noise Ratio vs Free-Air Temperature



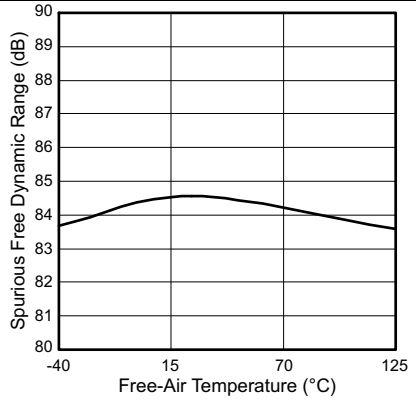
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 3 V
f_{input} = 100 kHz

Figure 22. Signal-to-Noise With Distortion vs Free-Air Temperature



f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 3 V
f_{input} = 100 kHz

Figure 23. Total Harmonic Distortion vs Free-Air Temperature



f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 3 V
f_{input} = 100 kHz

Figure 24. Spurious-Free Dynamic Range vs Free-air Temperature

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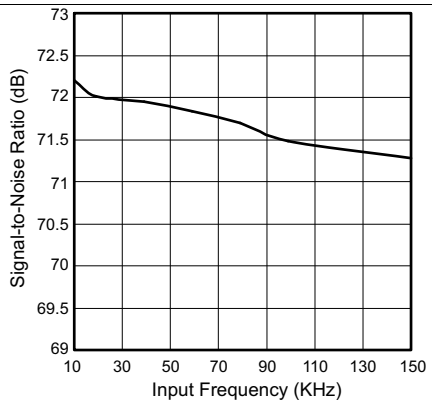
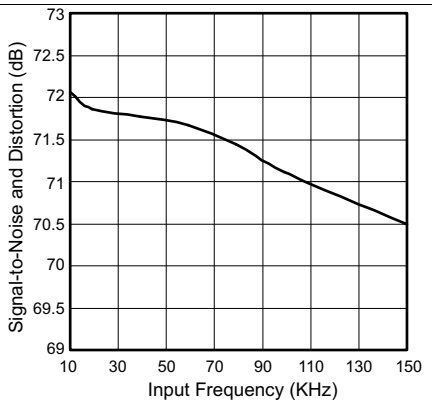
Typical Characteristics (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves.



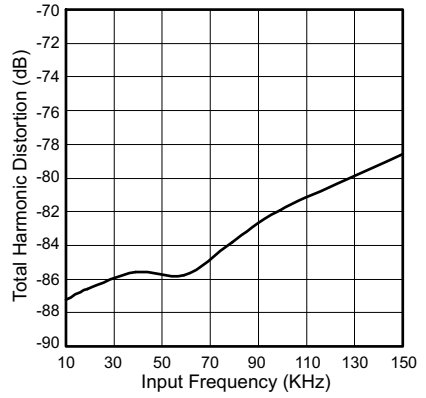
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 3 V
T_A = 25°C MXO shorted to AINP

Figure 25. Signal-to-Noise Ratio vs Input Frequency



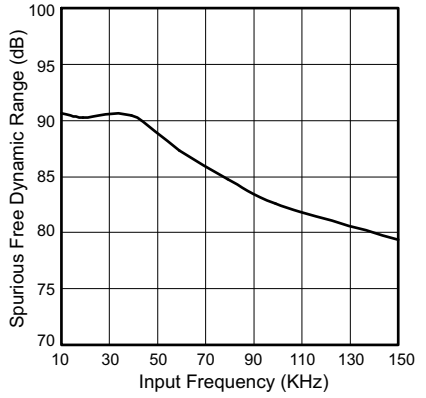
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 3 V
T_A = 25°C MXO shorted to AINP

Figure 26. Signal-to-Noise With Distortion vs Input Frequency



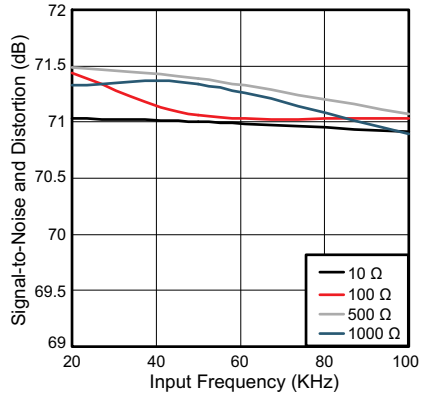
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 3 V
T_A = 25°C MXO shorted to AINP

Figure 27. Total Harmonic Distortion vs Input Frequency



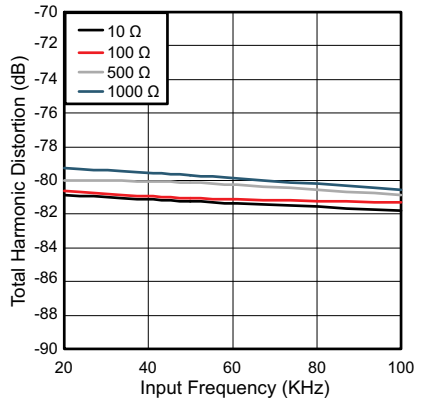
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 3 V
T_A = 25°C MXO shorted to AINP

Figure 28. Spurious-Free Dynamic Range vs Input Frequency



f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V
T_A = 25°C Buffer between MXO and AINP

Figure 29. Signal-to-Noise With Distortion vs Input Frequency (Across Different Source Resistance Values)



f_{sample}= 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V
T_A = 25°C Buffer between MXO and AINP

Figure 30. Total Harmonic Distortion vs Input Frequency (Across Different Source Resistance Values)

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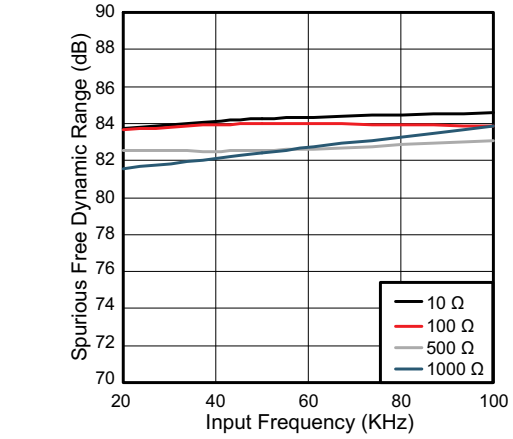
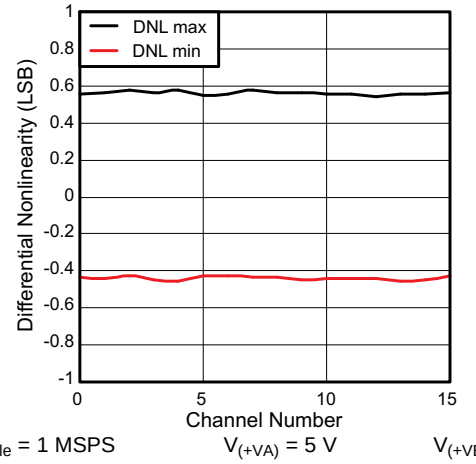
Typical Characteristics (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves.



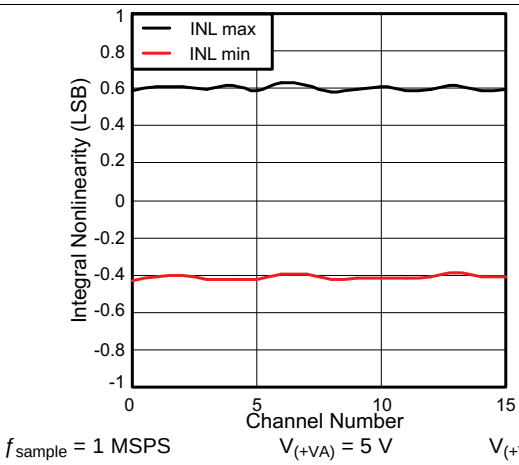
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V
T_A = 25°C Buffer between MXO and AINP

Figure 31. Spurious-Free Dynamic Range vs Input Frequency (Across Different Source Resistance Values)



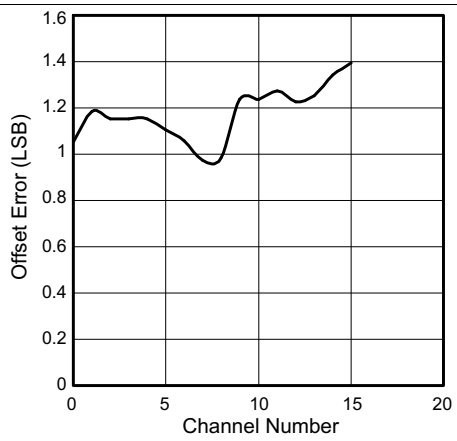
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V

Figure 32. Differential Nonlinearity Variation Across Channels



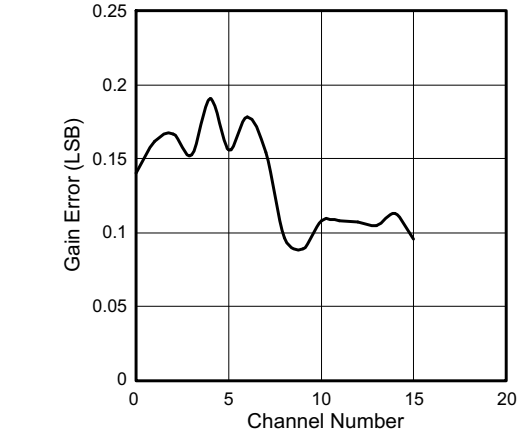
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V

Figure 33. Integral Nonlinearity Variation Across Channels



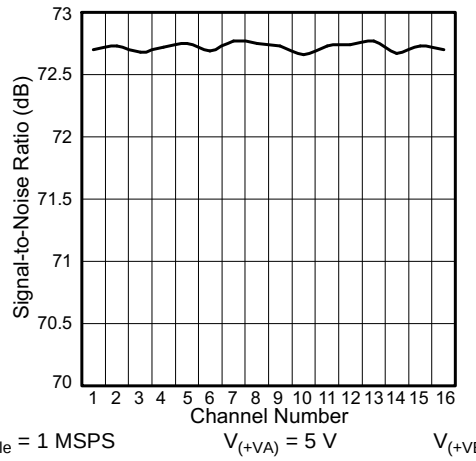
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V

Figure 34. Offset-Error Variation Across Channels



f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V

Figure 35. Gain-Error Variation Across Channels



f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V

Figure 36. Signal-to-Noise Ratio Variation Across Channels

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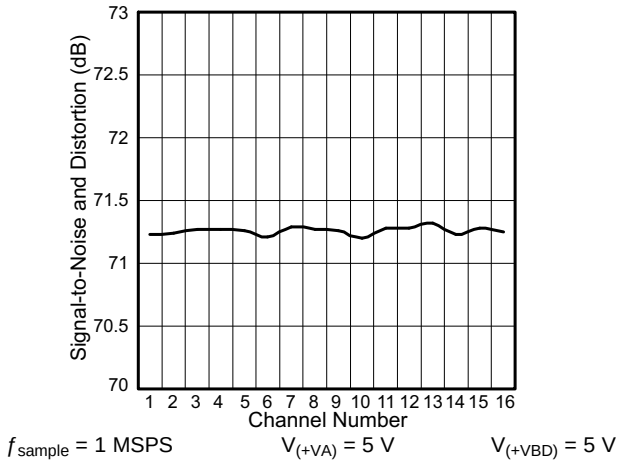
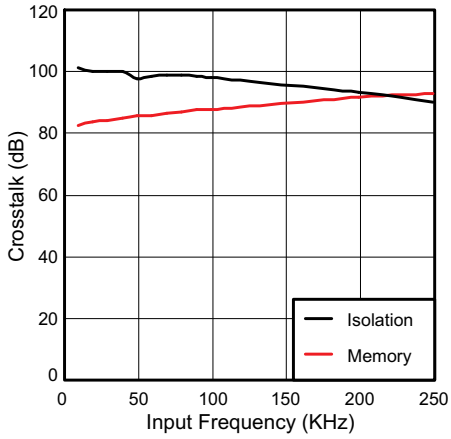
Typical Characteristics (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves.



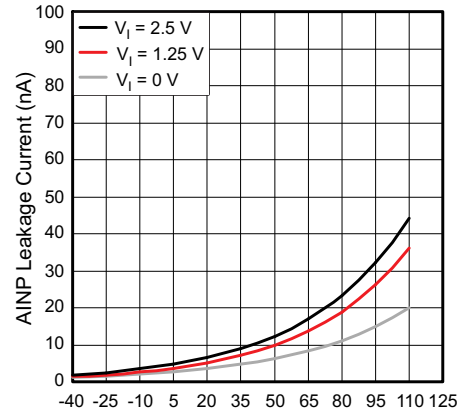
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V

Figure 37. Signal-to-Noise With Distortion Variation Across Channels



f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V
CH0, CH1

Figure 38. Crosstalk vs Input Frequency



$V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V

Figure 39. Input Leakage Current vs Free-Air Temperature

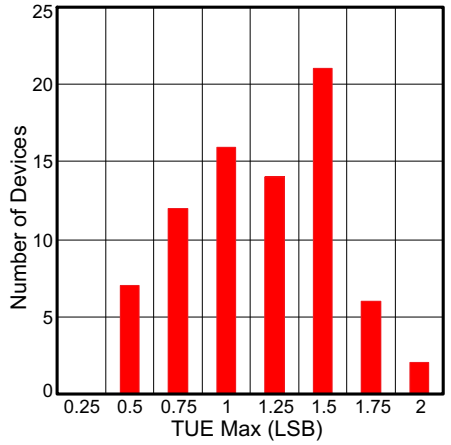


Figure 40. Total Unadjusted Error (TUE) Maximum

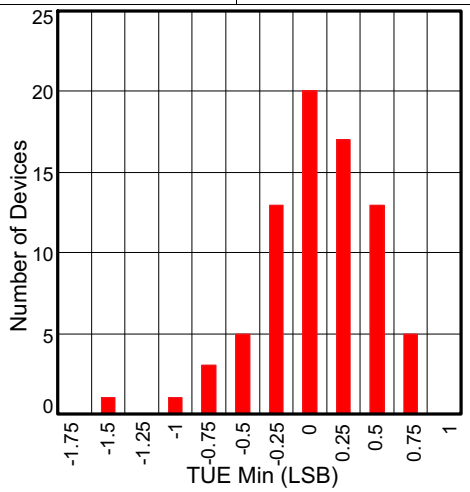


Figure 41. Total Unadjusted Error (TUE) Minimum

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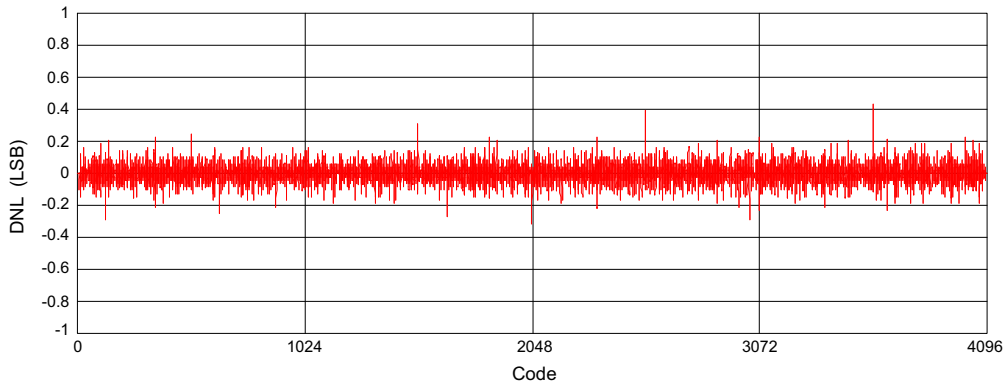
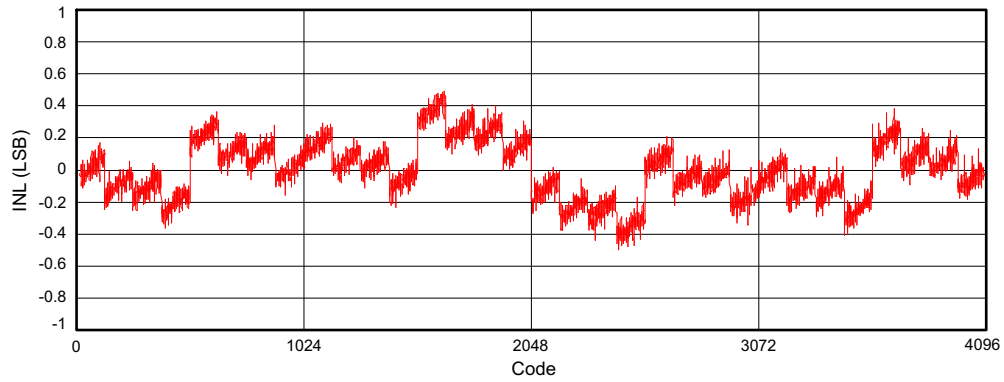


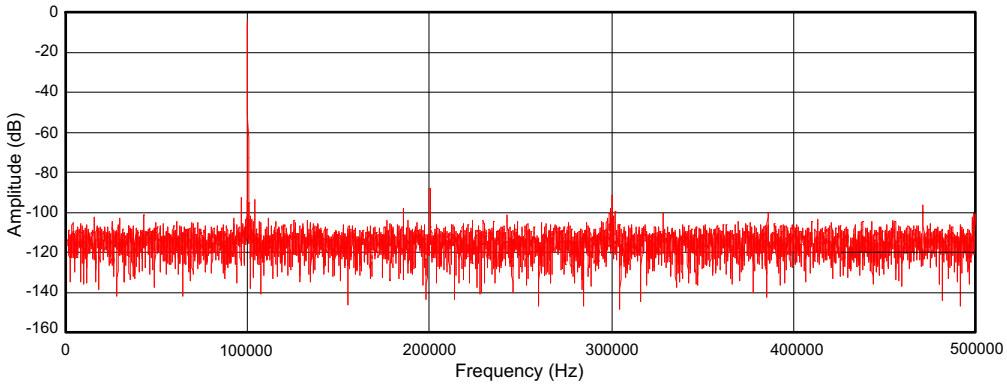
f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V
T_A = 25°C

Figure 42. Differential Linearity (DNL) Error



f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V

Figure 43. Integral Linearity (INL) Error



f_{sample} = 1 MSPS $V_{(+VA)}$ = 5 V $V_{(+VBD)}$ = 5 V
f_{input} = 100 kHz Npoints = 16,384

Figure 44. Power Spectrum

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8 Detailed Description

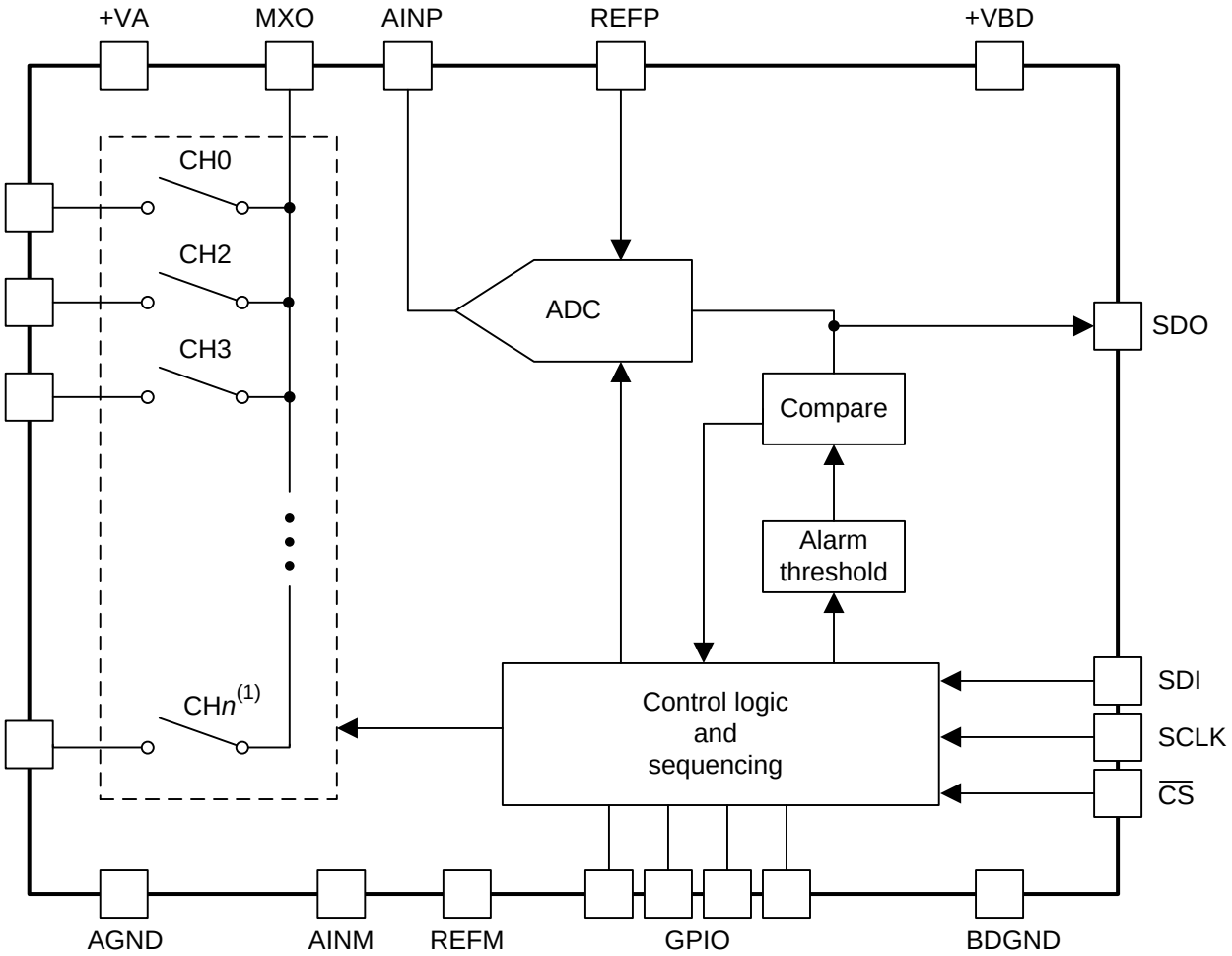
8.1 Overview

The ADS79xx-Q1 device is a high-speed, low-power analog-to-digital converter (ADC) with an 8-bit, 10-bit, and 12-bit multichannel successive-approximation register (SAR). The architecture of the device is based on charge redistribution, which includes a sample and hold function. The ADS79xx-Q1 device uses an external reference and an external serial clock (SCLK) to run the conversion.

The analog input is provided to the CHn input channel. The output of the multiplexer can be shorted directly or can be connected thorough a buffer to the AINP pin. Because the AINM pin is shorted to AGND, when a conversion is initiated, the differential input between the AINP and AGND pins is sampled on the internal capacitor array. Two input ranges are supported. Users can program the input range to either 0 V to V_{ref} or 0 V to 2 × V_{ref} using the mode-control register. The same register can program the input channel sequencing.

The ADS79xx-Q1 device also has four general-purpose input and output (GPIO) pins that can be programmed independently as either general-purpose output (GPO) or general-purpose Input (GPI) pins. GPIOs also support alarm function for which high and low thresholds are programmable per channel.

8.2 Functional Block Diagram



(1) *n* is number of channels (4, 8, 12, or 16) depending on the device from the ADS79xx-Q1 device family.

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8.3 Feature Description

8.3.1 Device Operation

Figure 45, Figure 46, Figure 47, and Figure 48 illustrate device operation timing. Device operation is controlled with the $\overline{CS}$, SCLK, and SDI pins. The device outputs data on the SDO pin.

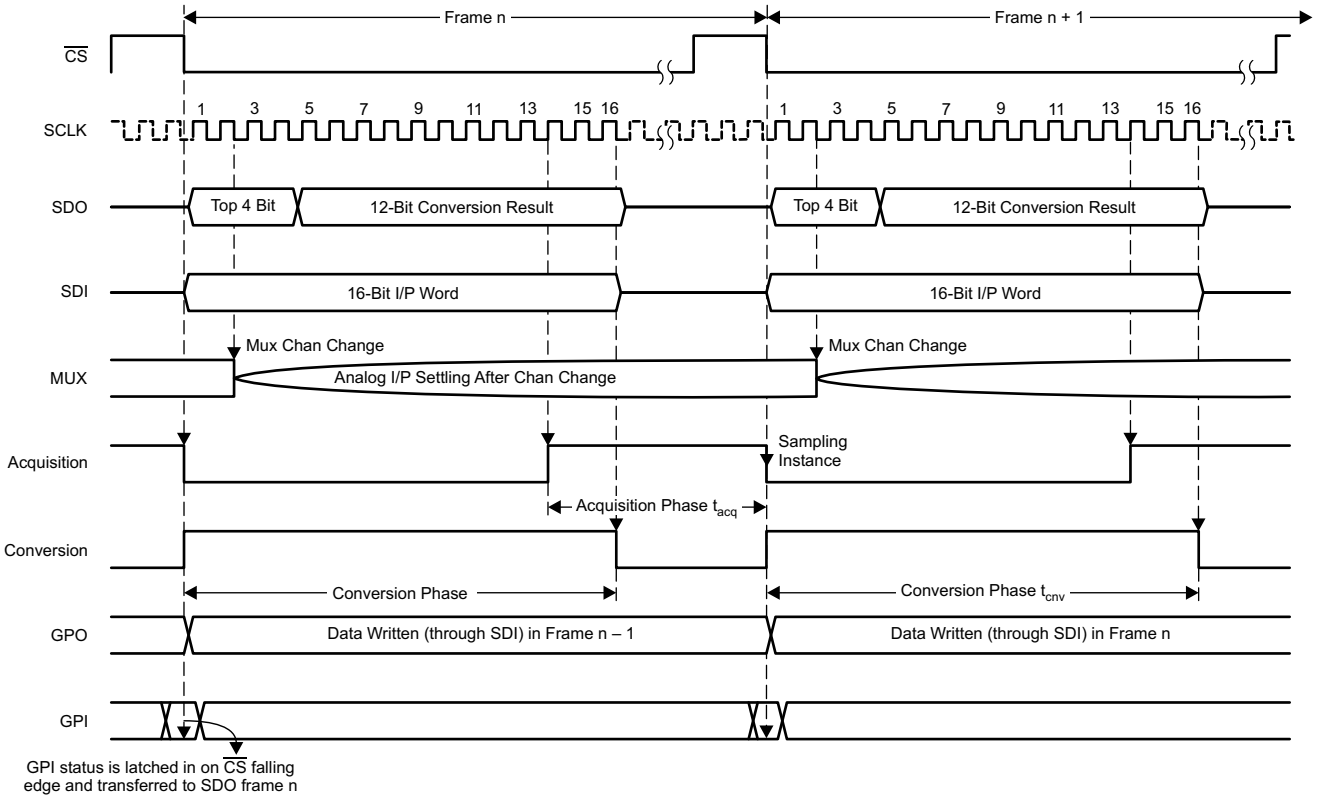

Figure 45. Device Operation Timing Diagram

Each frame begins with the falling edge of the $\overline{CS}$ pin. With the falling edge of the $\overline{CS}$ pin, the input signal from the selected channel is sampled, and the conversion process is initiated. The device outputs data while the conversion is in progress. The 16-bit data word contains a 4-bit channel address, followed by a 12-bit conversion result in most-significant-bit (MSB) first format. The GPIO status can be read instead of the channel address (see Table 1, Table 2, and Table 5).

The device selects a new multiplexer channel on the second SCLK falling edge. The acquisition phase begins on the 14th SCLK rising edge. On the next $\overline{CS}$ falling edge the acquisition phase ends, and the device starts a new frame.

There are four general-purpose IO (GPIO) pins. These pins can be individually programmed as GPO or GPI. Using these pins for preassigned functions is also possible (see Table 11). GPO data can be written into the device through the SDI line. The device refreshes the GPO data on the $\overline{CS}$ falling edge according to the SDI data written in previous frame.

Similarly the device latches the GPI status on the $\overline{CS}$ falling edge and outputs the GPI data on the SDO line (if GPI read is enabled by writing DI04 = 1 in the previous frame) in the same frame starting with the $\overline{CS}$ falling edge.

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Feature Description (continued)

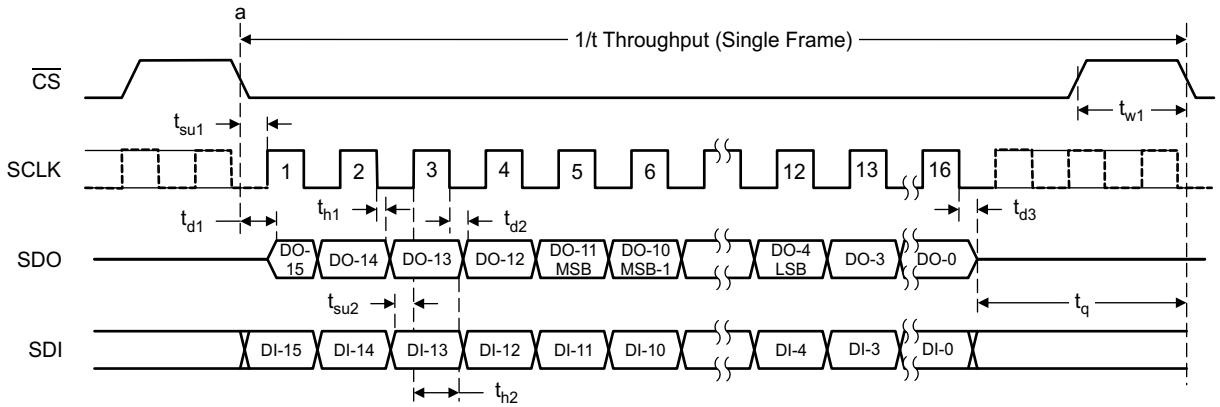

Figure 46. Serial Interface Timing Diagram for 8-Bit Devices (ADS7958, ADS7959, ADS7960, and ADS7961)

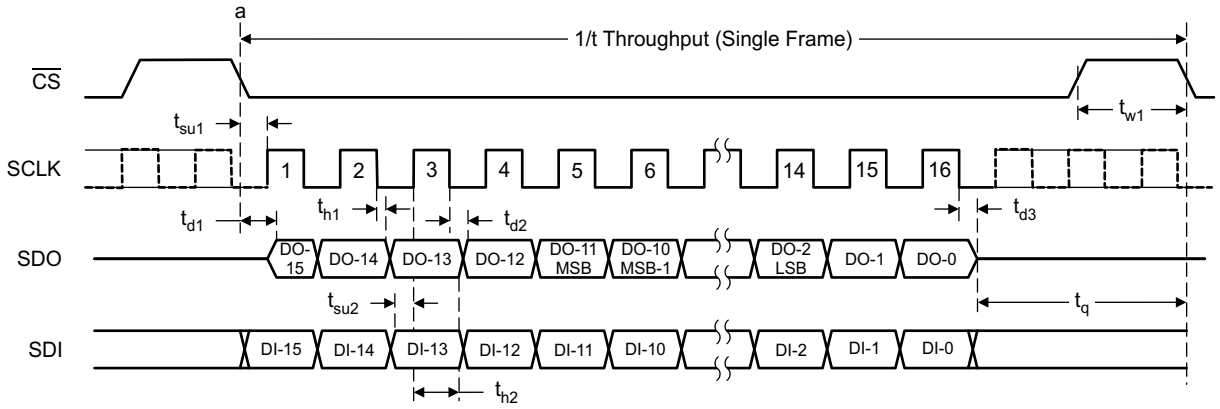

Figure 47. Serial Interface Timing Diagram for 10-Bit Devices (ADS7954, ADS7956, and ADS7957)

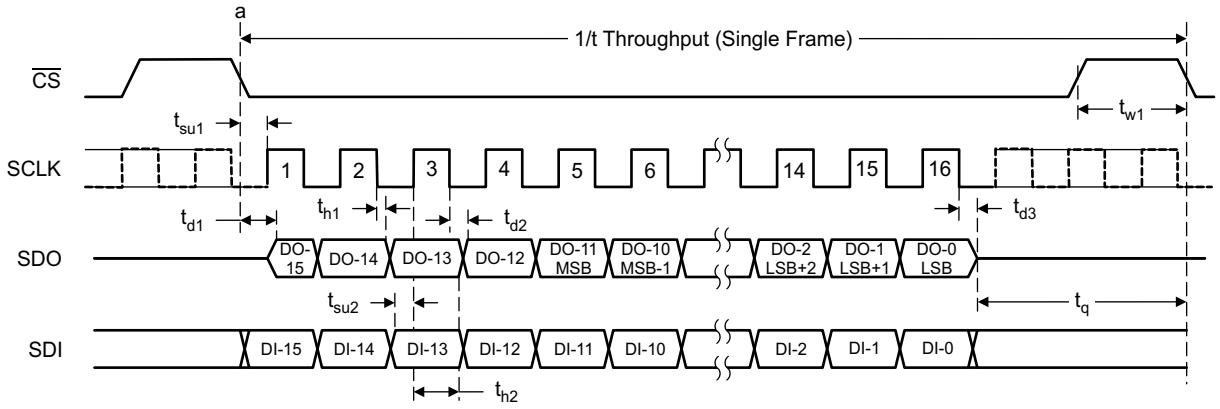

Figure 48. Serial Interface Timing Diagram for 12-Bit Devices (ADS7950, ADS7951, ADS7952, and ADS7953)

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Feature Description (continued)

The falling edge of the $\overline{CS}$ pin clocks out the DO-15 bit (the first bit of the four bit channel address), and remaining address bits are clocked out on every falling edge of SCLK until the third falling edge. The conversion result MSB is clocked out on the fourth SCLK falling edge and LSB on the 11th, 13th, or 15th falling edge respectively for 8-bit, 10-bit, or 12-bit devices. On the 16th falling edge of the SCLK pin, the SDO pin enters tri-state condition. The conversion ends on the 16th falling edge of SCLK.

While the device outputs data on the SDO pin, a 16-bit word is read on the SDI pin. The SDI data are latched on every rising edge of the SCLK pin beginning with the first clock; see Figure 46, Figure 47, and Figure 48.

The $\overline{CS}$ pin can be asserted (pulled high) only after 16 clocks have elapsed.

The device has two (high and low) programmable alarm thresholds per channel. If the input crosses these limits the device flags out an alarm on the GPIO0 or GPIO1 pin depending on the GPIO-program register settings (see Table 11). The alarm is asserted (under the alarm conditions) on the 12th falling edge of the SCLK pin in the same frame when a data conversion is in progress. The alarm output is reset on the tenth falling edge of the SCLK pin in the next frame.

8.3.2 Device Power-up Sequence

Figure 49 illustrates the device power-up sequence. Manual mode is the default power-up channel-sequencing mode and channel-0 is the first channel by default. As explained previously, these devices offer program registers to configure user-programmable features (such as GPIO, alarm, and to preprogram the channel sequence for the auto modes). At power up or on reset, these registers are set to the default values listed in Table 1 to Table 11. Program these registers on power up or after reset. When configured, the device is ready to use in any of the three channel sequencing modes: manual, auto-1, and auto-2.

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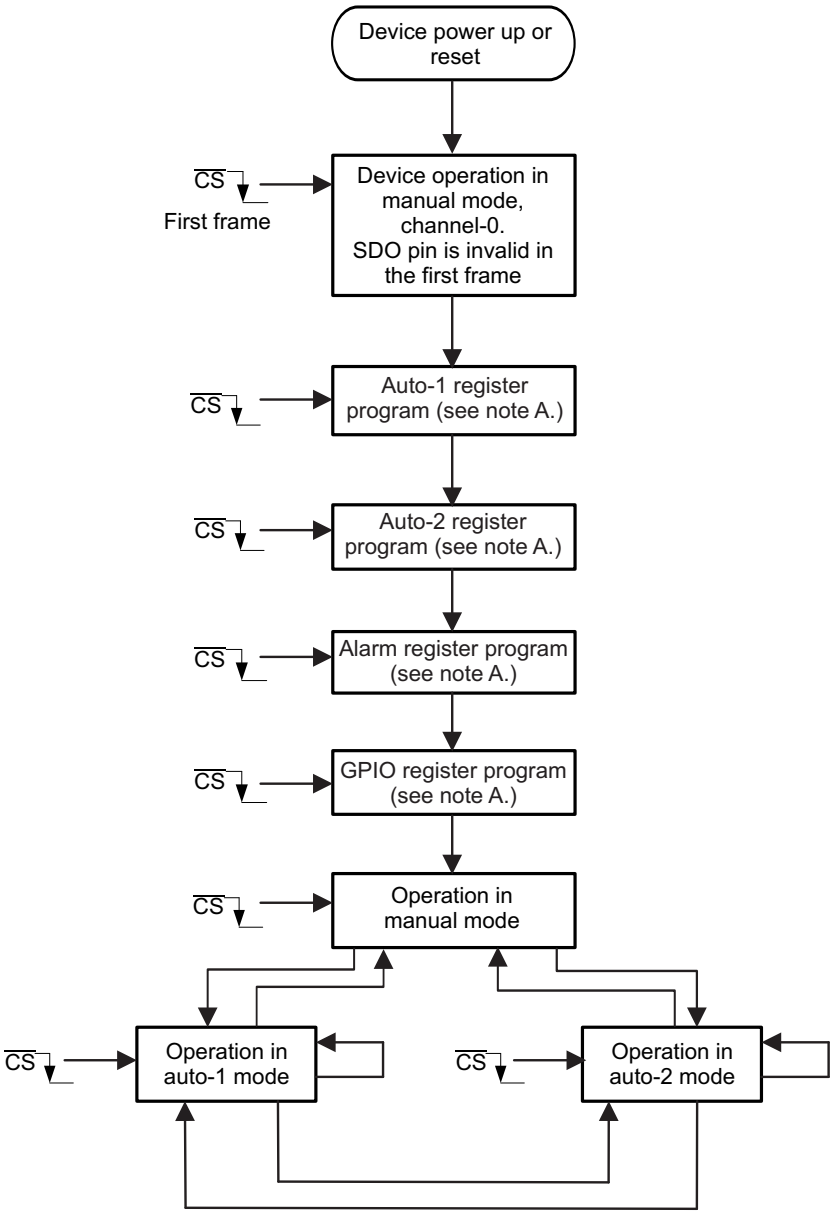
Feature Description (continued)



A. The device continues operation in manual-mode channel 0 throughout the programming sequence and outputs valid conversion results. Changing the channel, range, or GPIO is possible by inserting extra frames in between two programming blocks. Bypassing any programming block is also possible if that feature in not intended for use.

B. Reprogramming the device at any time during operation, regardless of what mode the device is in, is possible. During programming, the device continues operation in whatever mode it is in and outputs valid data.

Figure 49. Device Power-Up Sequence

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Feature Description (continued)

8.3.3 Analog Input

The ADS79x-Q1 device family offers 8-bit, 10-bit, and 12-bit ADCs with 4-channel, 8-channel, 12-channel, 16-channel multiplexers for analog input. The multiplexer output is available on the MXO pin. The AINP pin is the ADC input pin. The devices offers flexibility for a system designer as both MXO and AINP are accessible externally.

Figure 50 shows the equivalent circuit at the input and output of the multiplexer and the input of the converter during sampling. When the converter enters hold mode, the input impedance at AINP is greater than 1 GΩ.

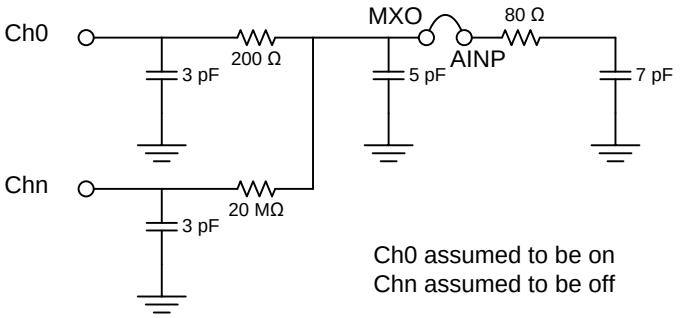

Figure 50. ADC and MUX Equivalent Circuit

When the converter samples an input, the voltage difference between the AINP and AGND pins is captured on the internal capacitor array. The peak input current through the analog inputs depends upon a number of factors including sample rate, input voltage, and source impedance. The current into the ADS79xx-Q1 device charges the internal capacitor array during the sample period. After this capacitance is fully charged, there is no further input current.

To maintain the linearity of the converter, the Ch0 through Chn and AINP inputs must be within the input range limits specified. Outside of these ranges, converter linearity may not meet specifications.

8.3.4 Reference

The ADS79xx-Q1 device can operate with an external 2.5-V ±10-mV reference. A clean, low-noise, well-decoupled reference voltage on the REF pin is required to ensure good performance from the converter. A low-noise, band-gap reference (such as the REF5025 device) can be used to drive this pin. A 10-µF ceramic decoupling capacitor is required between the REF and GND pins of the converter. Place the capacitor as close as possible to the device pins.

8.3.5 Power Saving

The ADS79xx-Q1 device offers a power-down feature to save power when not in use. There are two ways to power down the device. The device can be powered down by writing the DI05 bit equal to 1 in the mode control register (see Table 1, Table 2, and Table 5). In this case, the device powers down on the 16th falling edge of the SCLK pin in the next data frame. Another way to power down the device is through the GPIO pins. The GPIO3 pin can act as a $\overline{PD}$ input (see Table 11 for assigning this functionality to the GPIO3 pin) which is an asynchronous and active-low input. The device powers down instantaneously after the GPIO3 pin ($\overline{PD}$) equals 0. The device powers up again on the $\overline{CS}$ falling edge when the DI05 bit equals 0 in the mode control register, and the GPIO3 pin ($\overline{PD}$) equals 1.

8.4 Device Functional Modes

8.4.1 Channel Sequencing Modes

There are three modes for channel sequencing, including *manual mode*, *auto-1 mode*, and *auto-2 mode*. Mode selection occurs by writing into the *control register* (see Table 1, Table 2, and Table 5). A new multiplexer channel is selected on the second falling edge of SCLK (as shown in Figure 45) in all three modes.

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Device Functional Modes (continued)

Manual mode: When configured to operate in manual mode, the next selected channel is programmed in each frame and the device selects the programmed channel in the next frame. On power up or after reset the default channel is channel-0 and the device is in manual mode.

Auto-1 mode: In this mode the device scans pre-programmed channels in ascending order. A new multiplexer channel is selected every frame on the second falling edge of the SCLK pin. A separate program register preprograms the channel sequence. Table 3 and Table 4 show auto-1 program register settings.

When programmed, the device retains the program register settings until the device is powered down, reset, or reprogrammed. The device is allowed to exit and reenter the auto-1 mode any number of times without disturbing the program register settings.

The auto-1 program register is reset to F, FF, FFF, or FFFF (hex) for the 4-channel, 8-channel, 12-channel, or 16-channel devices, respectively, upon device power up or reset (implying the device scans all channels in ascending order).

Auto-2 mode: In this mode the user can configure the program register to select the last channel in the scan sequence. The device scans all channels from channel-0 up to, and including, the last channel in ascending order. The multiplexer channel is selected every frame on the second falling edge of the SCLK pin. A separate program register preprograms the last channel in the sequence (multiplexer depth). Table 6 lists the auto-2 program register settings for selection of the last channel in the sequence.

When programmed, the device retains the program register settings until the device is powered down, reset, or reprogrammed. The device is allowed to exit and re-enter auto-2 mode any number of times, without disturbing the program register settings.

On power up or reset, bits D9 to D6 of the auto-2 program register are reset to 3, 7, B, or F (hex) 4-channel, 8-channel, 12-channel or 16-channel devices, respectively (implying the device scans all channels in ascending order).

8.4.2 Device Programming and Mode Control

The following sections describe device programming and mode control. The ADS79xx-Q1 device feature two types of registers to configure and operate the devices in different modes. These registers are referred as configuration registers. The two types of configuration registers are mode control registers and program registers.

8.4.2.1 Mode Control Register

A mode control register is configured to operate the device in one of three channel sequencing modes, either manual mode, auto-1 mode, or auto-2 mode. This register is also used to control user programmable features, such as range selection, device power-down control, GPIO read control, and writing output data into the GPIO pins.

8.4.2.2 Program Registers

The program registers are used for device-configuration settings and are typically programmed once on power up or after device reset. There are different program registers including auto-1 mode programming for preprogramming the channel sequence, auto-2 mode programming for selection of the last channel in the sequence, alarm programming for all 16 channels (or 4, 8 , or 12 channels depending on the device), and GPIO for individual pin configuration, such as GPI or GPO or a preassigned function.

8.4.3 Operating In Manual Mode

Figure 51 illustrates details regarding entering and running in manual channel-sequencing mode. Table 1 lists the mode control register settings for manual mode in detail. Note that there are no program registers for manual mode.

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Device Functional Modes (continued)

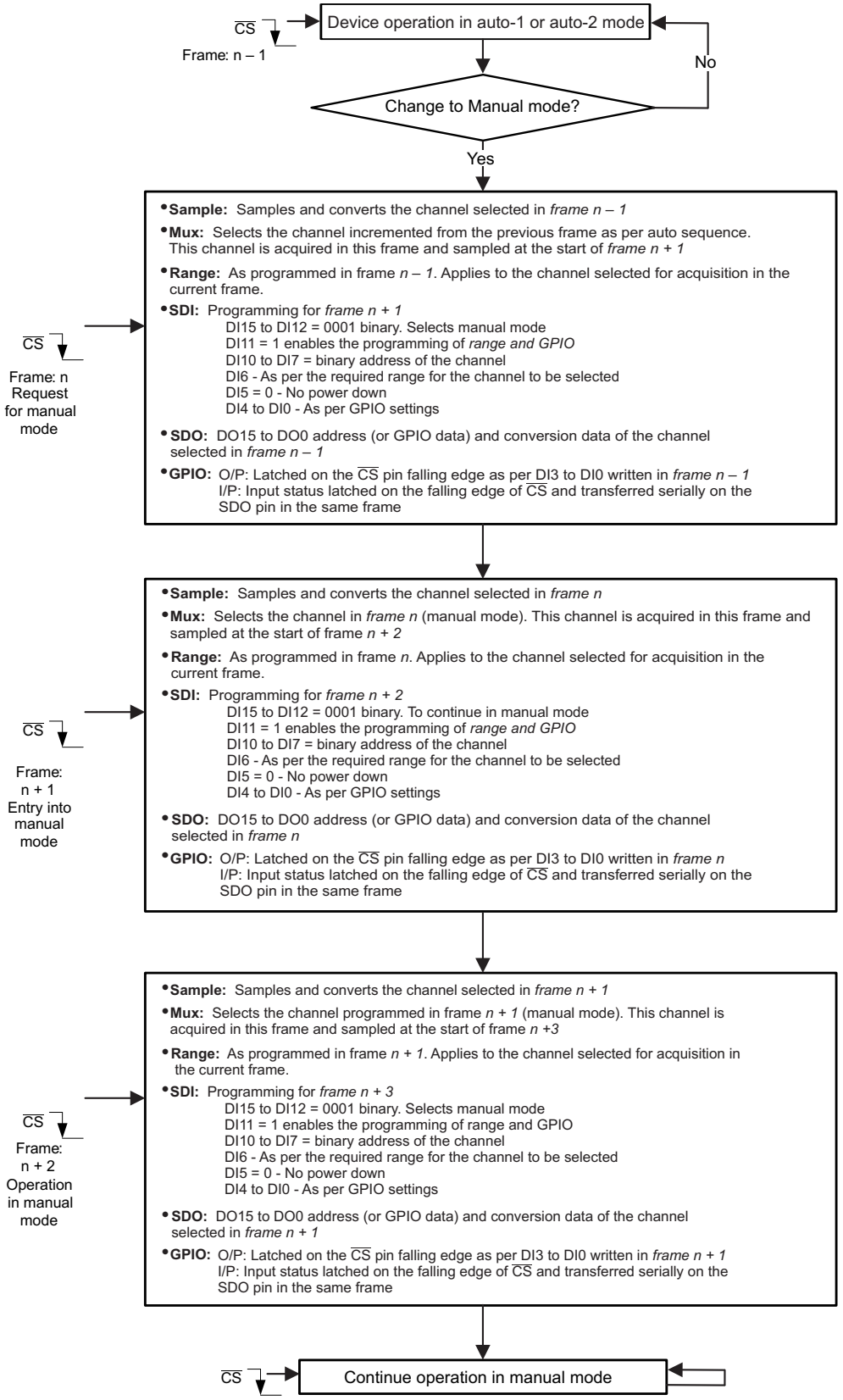

Figure 51. Entering and Running in Manual Channel-Sequencing Mode

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Device Functional Modes (continued)

Table 1. Mode-Control Register Settings for Manual Mode

BITS	RESET STATE	DESCRIPTION				
		LOGIC STATE	FUNCTION			
DI15-12	0001	0001	Selects manual mode			
DI11	0	1	Enables programming of bits DI06 through DI00			
		0	Device retains values of bits DI06 through DI00 from the previous frame			
DI10-07	0000	This 4-bit data represents the address of the next channel to be selected in the next frame. DI10 = MSB and DI07 = LSB. For example, 0000 represents channel-0, 0001 represents channel-1, and so on.				
DI06	0	0	Selects 2.5-V input range (range 1)			
		1	Selects 5-V input range (range 2)			
DI05	0	0	Device normal operation (no power down)			
		1	Device powers down on 16th SCLK falling edge			
DI04	0	0	The SDO pin outputs the current channel address of the channel on bits DO15 through DO12 followed by a 12-bit conversion result on bits DO11 through DI00.			
		1	The GPIO3 through GPIO0 data (both input and output) is mapped onto bits DO15 through DO12 in the order shown below. Lower data bits DO11 through DO00 represent the 12-bit conversion result of the current channel.			
			DOI5	**DOI4**	**DOI3**	**DOI2**
			GPIO3	GPIO2	GPIO1	GPIO0
DI03-00	0000	The GPIO data for the channels configured as an output. The device ignores the data for the channel which is configured as input. The SDI bit and corresponding GPIO information is given below.				
			DI03	**DI02**	**DI01**	**DI00**
			GPIO3	GPIO2	GPIO1	GPIO0

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8.4.4 Operating In Auto-1 Mode

Figure 52 shows a flowchart containing the details regarding entering and running in auto-1 channel-sequencing mode. Table 2 lists the mode control register settings for auto-1 mode in detail.

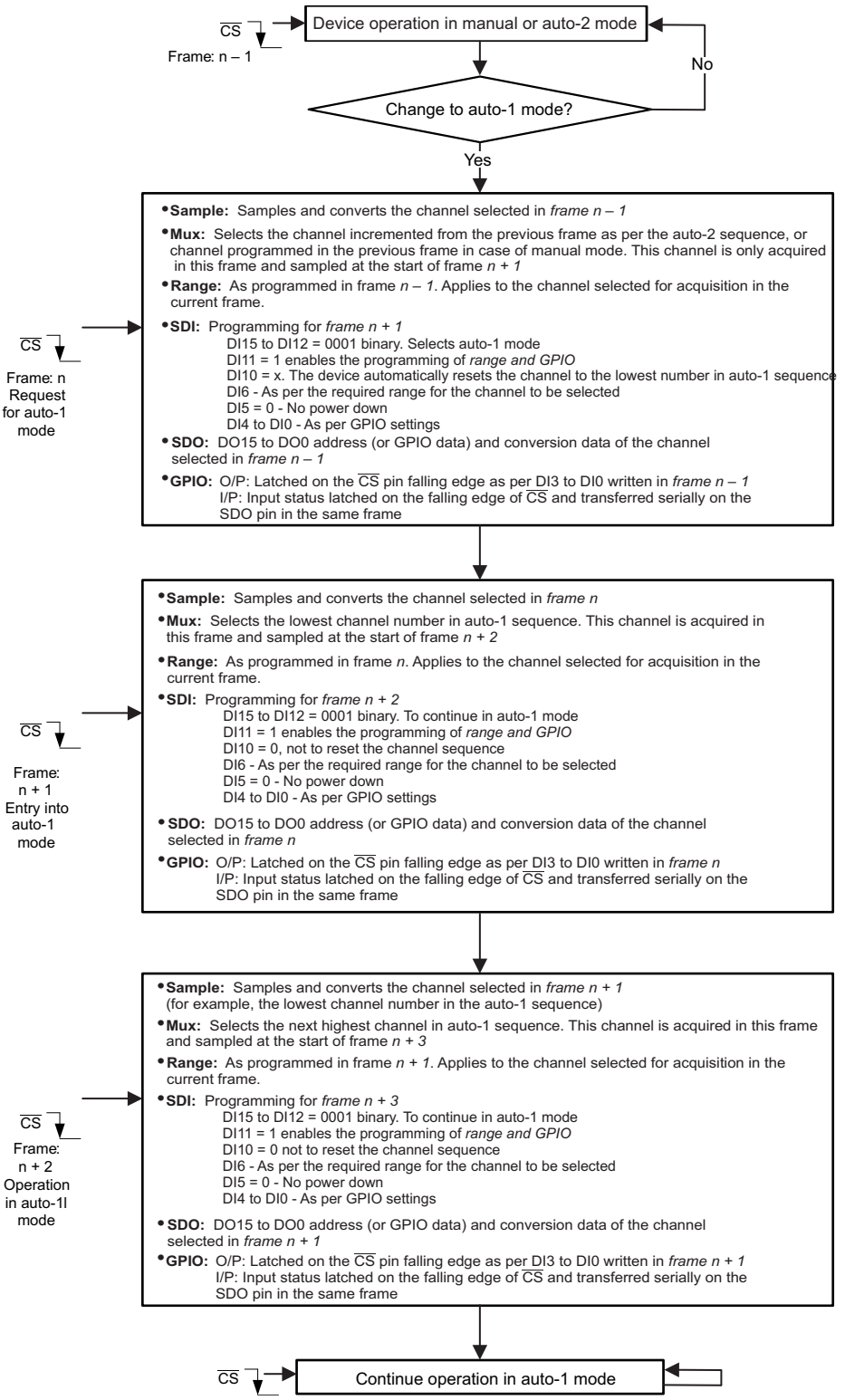

Figure 52. Entering and Running in Auto-1 Channel-Sequencing Mode

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Table 2. Mode-Control Register Settings for Auto-1 Mode

BITS	RESET STATE	DESCRIPTION				
		LOGIC STATE	FUNCTION			
DI15-12	0001	0010	Selects auto-1 mode			
DI11	0	1	Enables programming of bits DI10 through DI00			
		0	Device retains values of bits DI10 through DI00 from previous frame			
DI10	0	1	The channel counter is reset to the lowest programmed channel in the auto-1 program register			
		0	The channel counter increments every conversion (no reset)			
DI09-07	000	xxx	Do not care			
DI06	0	0	Selects 2.5-V input range (range 1)			
		1	Selects 5-V input range (range 2)			
DI05	0	0	Device normal operation (no powerdown)			
		1	Device powers down on the 16th SCLK falling edge			
DI04	0	0	SDO outputs current channel address of the channel on DO15..12 followed by 12-bit conversion result on DO11 through DO00.			
		1	The GPIO3 to GPIO0 data (both input and output) is mapped onto DO15 through DO12 in the order shown below. Lower data bits DO11 through DO00 represent the 12-bit conversion result of the current channel.			
			DO15	**DO14**	**DO13**	**DO12**
			GPIO3	GPIO2	GPIO1	GPIO0
DI03-00	0000	The GPIO data for the channels configured as an output. The device ignores the data for the channel which is configured as input. The SDI bit and corresponding GPIO information is given below				
			DI03	**DI02**	**DI01**	**DI00**
			GPIO3	GPIO2	GPIO1	GPIO0

The auto-1 program register is programmed (once on power up or reset) to preselect the channels for the auto-1 sequence, as shown in Figure 53. The auto-1 program-register programming requires two $\overline{CS}$ frames for complete programming. In the first $\overline{CS}$ frame, the device enters the auto-1 register programming sequence, and in the second frame the device programs the auto-1 program register. For complete details see Table 2, Table 3, and Table 4.

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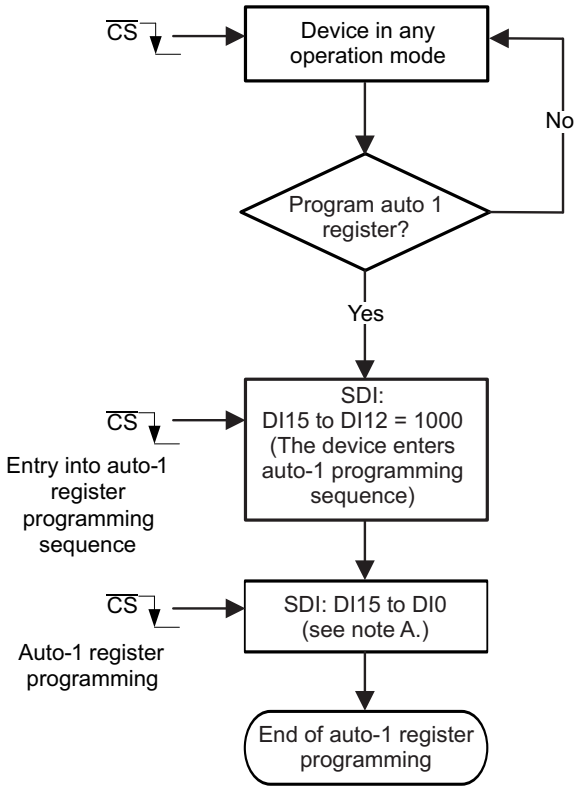

A. Per Table 3 and Table 4.

B. The device continues operation in the selected mode during programming. The SDO pin is valid, however changing the range or writing the GPIO data into the device during programming is not possible.

Figure 53. Auto-1 Register Programming Flowchart

Table 3. Program Register Settings for Auto-1 Mode

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
FRAME 1			
DI15-12	NA	1000	The device enters auto-1 program sequence. Device programming occurs in the next frame.
DI11-00	NA	Do not care	
FRAME 2			
DI15-00	All 1's	1 (individual bit)	A particular channel is programmed to be selected in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits. For example, DI15 → Ch15, DI14 → Ch14 … DI00 → Ch00
		0 (individual bit)	A particular channel is programmed to be skipped in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits. For example, DI15 → Ch15, DI14 → Ch14 … DI00 → Ch00

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Table 4. Mapping of Channels to SDI Bits

DEVICE(1)	SDI BITS															
	DI15	DI14	DI13	DI12	DI11	DI10	DI09	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01	DI00
4 Channel	X	X	X	X	X	X	X	X	X	X	X	X	1/0	1/0	1/0	1/0
8 Channel	X	X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
12 Channel	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
16 Channel	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

(1) When operating in auto-1 mode, the device only scans the channels programmed to be selected.

8.4.5 Operating In Auto-2 Mode

Figure 54 illustrates the details regarding entering and running in auto-2 channel-sequencing mode. Table 5 lists the mode-control register settings for auto-2 mode in detail.

Table 5. Mode-Control Register Settings for Auto-2 Mode

BITS	RESET STATE	DESCRIPTION				
		LOGIC STATE	FUNCTION			
DI15-12	0001	0011	Selects auto-2 mode			
DI11	0	1	Enables programming of bits DI10 through DI00			
		0	The device retains values of DI10 through DI00 from the previous frame			
DI10	0	1	The channel number is reset to Ch-00			
		0	The channel counter increments every conversion (no reset)			
DI09-07	000	xxx	Do not care			
DI06	0	0	Selects 2.5-V input range (range 1)			
		1	Selects 5-V input range (range 2)			
DI05	0	0	Device normal operation (no powerdown)			
		1	The device powers down on the 16th SCLK falling edge			
DI04	0	0	The SDO pin outputs the current channel address of the channel on bits DO15 through DO12 followed by the 12-bit conversion result on bits DO11 through DO00.			
		1	The GPIO3 to GPIO0 data (both input and output) is mapped onto bits DO15 through DO12 in the order shown below. Lower data bits DO11 through DO00 represent the 12-bit conversion result of the current channel.			
			DO15	**DO14**	**DO13**	**DO12**
			GPIO3	GPIO2	GPIO1	GPIO0
DI03-00	0000	The GPIO data for the channels configured as an output. The device ignores data for the channel that is configured as input. The SDI bit and corresponding GPIO information is given below.				
			DI03	**DI02**	**DI01**	**DI00**
			GPIO3	GPIO2	GPIO1	GPIO0

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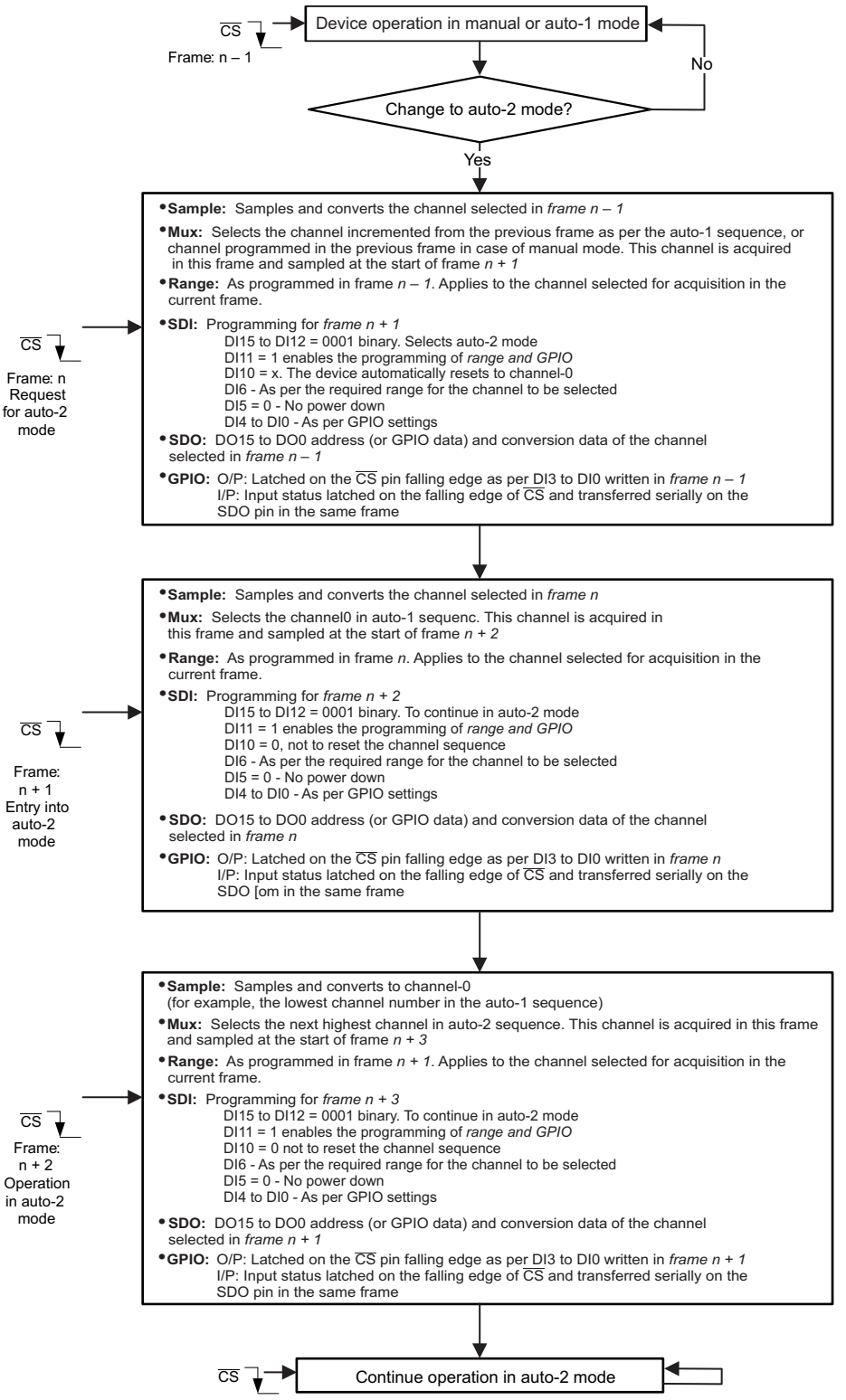
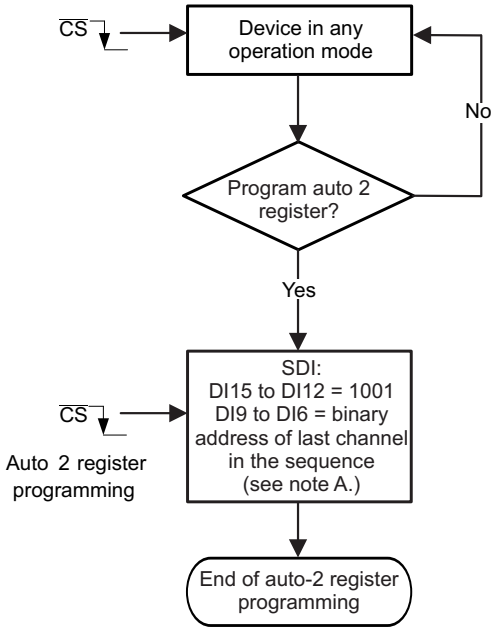


Figure 54. Entering and Running in Auto-2 Channel-Sequencing Mode

The auto-2 program register is programmed (once on power up or reset) to preselect the last channel (or sequence depth) in the auto-2 sequence. Unlike auto-1 program-register programming, auto-2 program-register programming requires only one $\overline{CS}$ frame for complete programming. Figure 55 and Table 6 provide complete details.



A. See Table 6.

B. The device continues operation in the selected mode during programming. The SDO pin is valid, however changing the range or writing the GPIO data into the device during programming is not possible.

Figure 55. Auto-2 Register Programming Flowchart

Table 6. Program Register Settings for Auto-2 Mode

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
DI15-12	NA	1001	The auto-2 program register is selected for programming
DI11-10	NA	Do not care	
DI09-06	NA	aaaa	This 4-bit data represents the address of the last channel in the scanning sequence. During device operation in auto-2 mode, the channel counter begins at CH-00 and increments every frame until the counter equals *aaaa*. The channel counter then rolls over to CH-00 in the next frame.
DI05-00	NA	Do not care	

8.4.6 Continued Operation In A Selected Mode

When a device is programmed to operate in one of the modes, the user can continue to operate in the same mode. Table 7 lists mode-control register settings to continue operating in a selected mode.

Table 7. Continued Operation in a Selected Mode

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
DI15-12	0001	0000	The device continues to operate in the selected mode. In auto-1 and auto-2 modes the channel counter increments normally, whereas in the manual mode the device continues with the last selected channel. The device ignores data on bits DI11-DI00 and continues operating as per the previous settings. This feature is provided so that the SDI pin can be held low when no changes are required in the mode-control register settings.
DI11-00	All 0	The device ignores these bits when bit DI15-12 is set to 0000 logic state	

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8.5 Digital Output Code

As discussed previously in the *Device Operation* section, the digital output of the ADS79xx-Q1 devices is SPI™ compatible. Table 8, Table 9, and Table 10 list the output codes corresponding to various analog input voltages.

Table 8. Ideal Input Voltages and Output Codes for 8-Bit Devices (ADS7958, ADS7959, ADS7960, and ADS7961)

DESCRIPTION	ANALOG VALUE		DIGITAL OUTPUT STRAIGHT BINARY	
			BINARY CODE	HEX CODE
Full-scale range	Range 1 → V_{ref}	Range 2 → 2 × V_{ref}	—	—
Least-significant bit (LSB)	V_{ref} / 256	2 × V_{ref} / 256	—	—
Full scale	V_{ref} – 1 LSB	2 × V_{ref} – 1 LSB	1111 1111	FF
Midscale	V_{ref} / 2	V_{ref}	1000 0000	80
Midscale – 1 LSB	V_{ref} / 2 – 1 LSB	V_{ref} – 1 LSB	0111 1111	7F
Zero	0 V	0 V	0000 0000	00

Table 9. Ideal Input Voltages and Output Codes for 10-Bit Devices (ADS7958, ADS7959, ADS7960, and ADS7961)

DESCRIPTION	ANALOG VALUE		DIGITAL OUTPUT STRAIGHT BINARY	
			BINARY CODE	HEX CODE
Full-scale range	Range 1 → V_{ref}	Range 2 → 2 × V_{ref}	—	—
Least-significant bit (LSB)	V_{ref} / 1024	2 × V_{ref} / 1024	—	—
Full scale	V_{ref} – 1 LSB	2 V_{ref} – 1 LSB	11 1111 1111	3FF
Midscale	V_{ref} / 2	V_{ref}	10 0000 0000	200
Midscale – 1 LSB	V_{ref} / 2 – 1 LSB	V_{ref} – 1 LSB	01 1111 1111	1FF
Zero	0 V	0 V	00 0000 0000	000

Table 10. Ideal Input Voltages and Output Codes for 12-Bit Devices (ADS7950, ADS7951, ADS7952, and ADS7953)

DESCRIPTION	ANALOG VALUE		DIGITAL OUTPUT STRAIGHT BINARY	
			BINARY CODE	HEX CODE
Full-scale range	Range 1 → V_{ref}	Range 2 → 2 × V_{ref}	—	—
Least-significant bit (LSB)	V_{ref} / 4096	2 × V_{ref} / 4096	—	—
Full scale	V_{ref} – 1 LSB	2 × V_{ref} – 1 LSB	1111 1111 1111	FFF
Midscale	V_{ref} / 2	V_{ref}	1000 0000 0000	800
Midscale – 1 LSB	V_{ref} / 2 – 1 LSB	V_{ref} – 1 LSB	0111 1111 1111	7FF
Zero	0 V	0 V	0000 0000 0000	000

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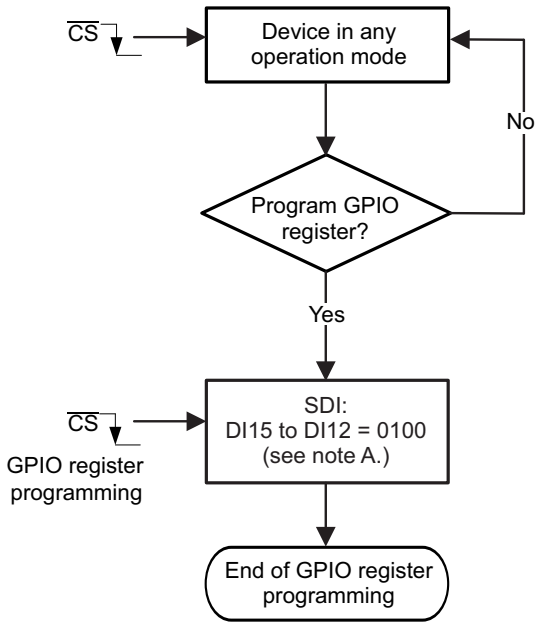
8.6 Programming: GPIO

8.6.1 GPIO Registers

The device has four general-purpose input and output (GPIO) pins. Each of the four pins can be independently programmed as general purpose output (GPO) or general purpose input (GPI). Using the GPIOs pins for some preassigned functions (see Table 11) is possible. The GPO data can be written into the device through the SDI line. The device refreshes the GPO data on every $\overline{CS}$ falling edge as per the SDI data written in the previous frame. Similarly, the device latches the GPI status on the $\overline{CS}$ falling edge and outputs it on the SDO pin (if the GPI pin is read-enabled by writing bit DI04 equal to 1 during the previous frame) in the same frame starting on the $\overline{CS}$ falling edge.

Figure 56 shows the details regarding programming the GPIO registers. Table 11 lists the details regarding GPIO-register programming settings.



A. See Table 12 for DI11 to DI00 data.

B. The device continues its operation in selected mode during programming. SDO is valid, however changing the range or writing GPIO data into the device during programming is not possible.

Figure 56. GPIO Program-Register Programming Flowchart

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Programming: GPIO (continued)

Table 11. GPIO Program-Register Settings

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
DI15-12	NA	0100	The device selects GPIO program registers for programming.
DI11-10	00	00	Do not program these bits to any logic state other than 00.
DI09	0	1	The device resets all registers in the next $\overline{CS}$ frame to the reset state shown in the corresponding tables (the device also resets itself).
		0	Device normal operation.
DI08	0	1	The device configures the GPIO3 pin as the device power-down input.
		0	The GPIO3 pin remains a general-purpose input or output.
DI07	0	1	The device configures the GPIO2 pin as a device-range input.
		0	The GPIO2 pin remains a general-purpose input or output.
DI06-04	000	000	The GPIO1 and GPIO0 pins remain a general-purpose input or output.
		xx1	The device configures the GPIO0 pin as a high-alarm or low-alarm output. This output is active high. GPIO1 remains general-purpose input or output.
		010	The device configures GPIO0 as a high-alarm output. This output is active high. The GPIO1 pin remains a general-purpose input or output.
		100	The device configures GPIO1 as a low-alarm output. This output is active high. The GPIO0 pin remains a general-purpose input or output.
		110	The device configures GPIO1 as a low-alarm output and the GPIO0 pin as a high-alarm output. These outputs are active high.
Note: The following settings are valid for the GPIO pins that are not assigned a specific function through bits DI08 to DI04			
DI03	0	1	The GPIO3 pin is configured as general-purpose output.
		0	The GPIO3 pin is configured as general-purpose input.
DI02	0	1	The GPIO2 pin is configured as general-purpose output.
		0	The GPIO2 pin is configured as general-purpose input.
DI01	0	1	The GPIO1 pin is configured as general-purpose output.
		0	The GPIO1 pin is configured as general-purpose input.
DI00	0	1	The GPIO0 pin is configured as general-purpose output.
		0	The GPIO0 pin is configured as general-purpose input.

8.6.2 Alarm Thresholds for GPIO Pins

Each channel has two alarm program registers, one for setting the high alarm threshold and the other for setting the low alarm threshold. For ease of programming, two alarm programming registers per channel, corresponding to four consecutive channels, are assembled into one group (a total of eight registers). There are four of these groups for 16-channel devices, and one, two or three of these groups for the 12-, 8-, or 4-channel devices, respectively. Table 12 lists the grouping of the various channels for each device in the ADS79xx-Q1 family. Figure 57 illustrates the details regarding programming the alarm thresholds. Table 13 lists the details regarding the alarm-program register settings.

Table 12. Grouping of Alarm Program Registers

GROUP NUMBER	REGISTERS	APPLICABLE FOR DEVICE
0	High and low alarm for channel 0, 1, 2, and 3	ADS750, ADS7952, ADS7951, and ADS7953; ADS7954, ADS7956, and ADS7957; ADS7958, ADS7959, ADS7960, and ADS7961
1	High and low alarm for channel 4, 5, 6, and 7	ADS7951, ADS7952, and ADS7953; ADS7956, and ADS7957; ADS7959, ADS7960, and ADS7961
2	High and low alarm for channel 8, 9, 10, and 11	ADS7953 and ADS7952, ADS7957 and ADS7956, ADS7961 and ADS7960
3	High and low alarm for channel 12, 13, 14, and 15	ADS7953, ADS7957, and ADS7961

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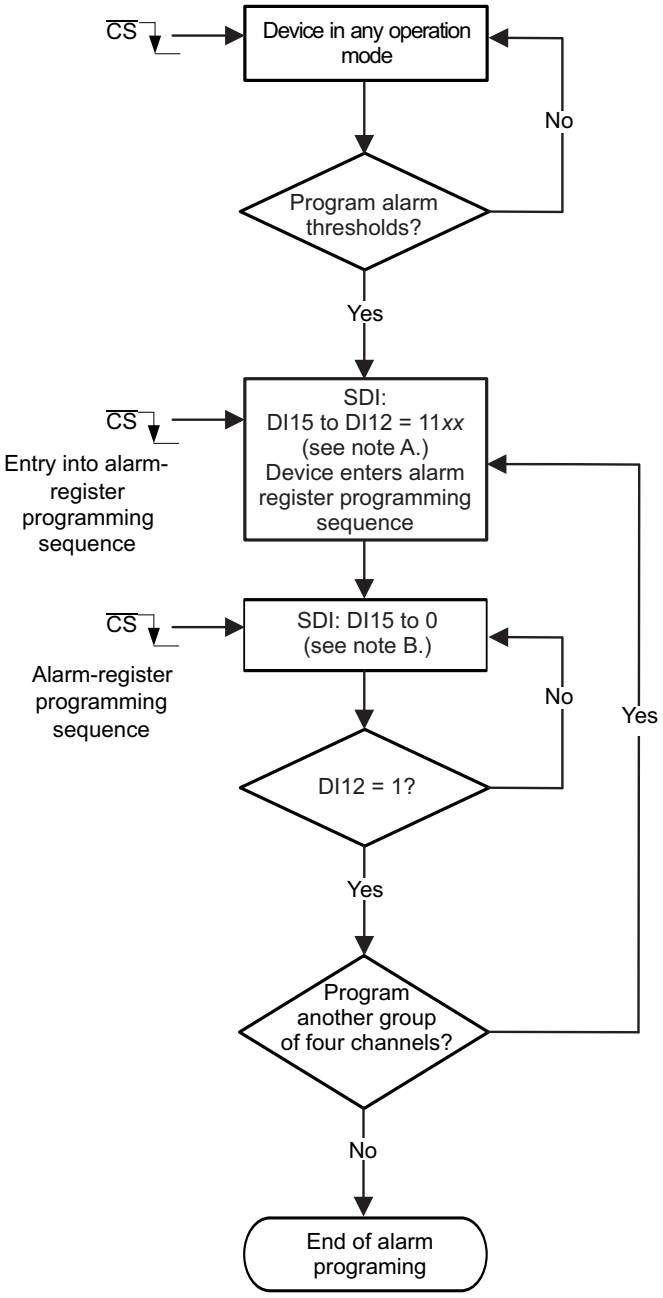
Each alarm group requires nine $\overline{CS}$ frames for programming the respective alarm thresholds. In the first frame the device enters the programming sequence and in each subsequent frame the device programs one of the registers from the group. The device offers a feature to program less than eight registers in one programming sequence. The device exits the alarm threshold programming sequence in the next frame after encountering the first exit alarm program bit high.



A. *xx* indicates a group of four channels (see Table 12).

B. Per Table 12.

C. The device continues operation in the selected mode during programming. The SDO pin is valid, however changing the range or writing the GPIO data into the device during programming is not possible.

Figure 57. Alarm Program Register Programming Flowchart

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Table 13. Alarm Program Register Settings

BITS	RESET STATE	DESCRIPTION	
		LOGIC STATE	FUNCTION
FRAME 1			
DI15-12	NA	1100	The device enters alarm programming sequence for group 0
		1101	The device enters alarm programming sequence for group 1
		1110	The device enters alarm programming sequence for group 2
		1111	The device enters alarm programming sequence for group 3
Note: Bits DI15-12 = 11*bb* is the alarm programming request for group *bb*. Here, *bb* represents the alarm programming group number in binary format.			
DI11-14	NA	Do not care	
FRAME 2 AND ONWARDS			
DI15-14	NA	*cc*	Where *cc* represents the lower two bits of the channel number in binary format. The device programs the alarm for the channel represented by the binary number *bbcc*. Note that *bb* is programmed in the first frame.
DI13	NA	1	High-alarm register selection
		0	Low-alarm register selection
DI12	NA	0	Continue alarm programming sequence in next frame
		1	Exit alarm programming in the next frame. **Note**: If the alarm programming sequence is not terminated using this feature then the device remains in the alarm programming sequence state and all SDI data is treated as alarm thresholds.
DI11-10	NA	xx	Do not care
DI09-00	All ones for high alarm register and all zeros for low alarm register	This 10-bit data represents the alarm threshold. The 10-bit alarm threshold is compared with the upper 10-bit word of the 12-bit conversion result. The device sets off an alarm when the conversion result is higher (high alarm) or lower (low alarm) than this number. For 10-bit devices, all 10 bits of the conversion result are compared with the set threshold. For 8-bit devices, all 8 bits of the conversion result are compared with DI09 to DI02 and DI00 and DI01 are *do not care*.	

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9 Application and Implementation

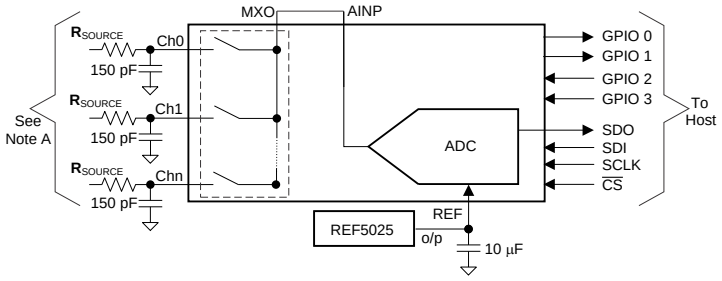
9.1 Application Information

In general applications, when the internal multiplexer is updated, the previously converted channel charge is stored in the 15-pF internal input capacitance that disturbs the voltage at the newly selected channel. This disturbance is expected to settle to 1 LSB during sampling (acquisition) time to avoid degrading converter performance. The initial absolute disturbance error at the channel input must be less than 0.5 V to prevent source current saturation or slewing that causes significantly long settling times. Fortunately, significantly reducing disturbance error is easy to accomplish by simply placing a large enough capacitor at the input of each channel. Specifically, with a 150-pF capacitor, instantaneous charge distribution keeps disturbance error below 0.46 V because the internal input capacitance can only hold up to 75 pC (or 5 V × 15 pF). The remaining error must be corrected by the voltage source at each input, with impedance low enough to settle within 1 LSB. The following application examples explain the considerations for the input source impedance (R_{SOURCE}).

9.2 Typical Applications

9.2.1 Unbuffered Multiplexer Output (MXO)

This application is the most typical application, but requires the lowest R_{SOURCE} for good performance. In this configuration, the 2xREF range allows larger source impedance than the 1xREF range because the 1xREF range LSB size is smaller, thus making it more sensitive to settling error.



A. A restriction on the source impedance exists. R_{SOURCE} ≤ 100 Ω for the 1xREF 12-bit settling at 1 MSPS or R_{SOURCE} ≤ 250 Ω for the 1xREF 12-bit settling at 1 MSPS .

Figure 58. Application Diagram for an Unbuffered MXO

9.2.1.1 Design Requirements

The design is optimized to show the input source impedance (R_{SOURCE}) between the 100 Ω to 10,000 Ω required to meet the 1-LSB settling at 12-bit, 10-bit, and 8-bit resolutions at different throughput in 1xREF (2.5-V) and 2xREF (5-V) input ranges.

9.2.1.2 Detailed Design Procedure

Although the required input source impedance can be estimated assuming a 0.5-V initial error and exponential recovery during sampling (acquisition) time, this estimation over-simplifies the complex interaction between the converter and source, thus yielding inaccurate estimates. Thus, this design uses an iterative approach with the converter itself to provide reliable impedance values.

To determine the actual maximum source impedance for a particular resolution and sampling rate, two subsequent channels are set at least 95% of the full-scale range apart. With a 1xREF range and 2.5 V_{ref}, the channel difference is at least 2.375 V. With 2xREF and 2.5 V_{ref}, the difference is at least 4.75 V. With a source impedance between 100 Ω to 10,000 Ω, the conversion runs at a constant rate and a channel update is issued that captures the first couple samples after the update. This process is repeated at least 100 times to remove any noise and to show a clear settling error. The first sample after the channel update is then compared against the second one. If the first and second samples are more than 1 LSB apart, throughput rate is reduced until the settling error becomes 1 LSB, which then sets the maximum throughput for the selected impedance. The whole process is repeated for nine different impedances between 100 Ω to 10,000 Ω.

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Typical Applications (continued)

9.2.1.3 Application Curves

These curves show the R_{SOURCE} for an unbuffered MXO.

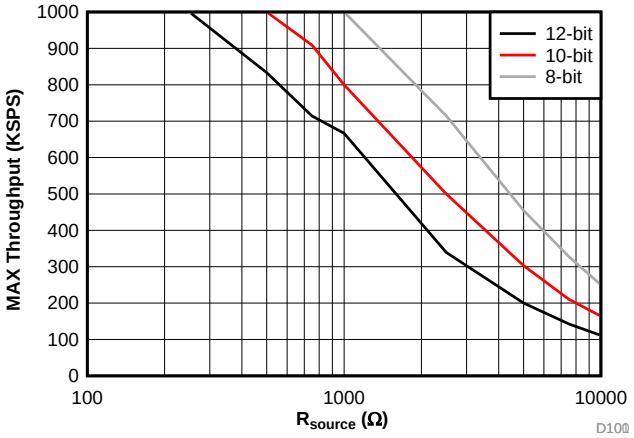


Figure 59. 2xREF Input Range Settling without an MXO Buffer

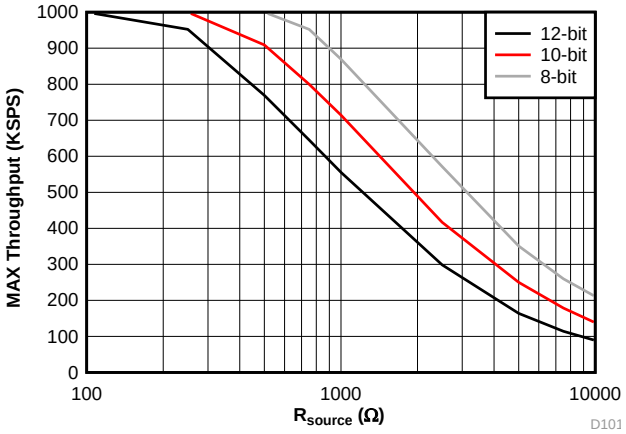
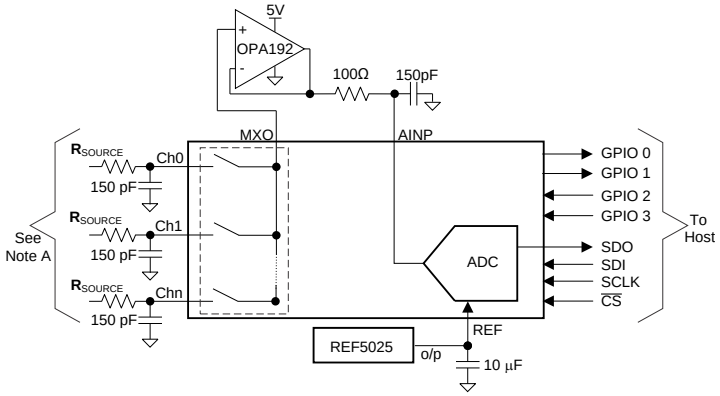


Figure 60. 1xREF Input Range Settling without an MXO Buffer

9.2.2 OPA192 Buffered Multiplexer Output (MXO)

The use of a buffer relaxes the R_{SOURCE} requirements to an extent. Charge from the sample-and-hold capacitor no longer dominates as a residual charge from a previous channel. Although having good performance is possible with a larger impedance using the OPA192, the output capacitance of the MXO also holds the previous channel charge and cannot be isolated, which limits how large the input impedance can finally be for good performance. In this configuration, the 1xREF range allows slightly higher impedance because the OPA192 (20 V/µs) slews approximately 2.5 V in contrast to the 2xREF range that requires the OPA192 to slew approximately 5 V.



A. Restriction on the source impedance exists. $R_{(SOURCE)} \leq 500\ \Omega$ for a 12-bit settling at 1 MSPS with both 1xREF and 2xREF ranges.

Figure 61. Application Diagram for an OPA192 Buffered MXO

9.2.2.1 Design Requirements

The design is optimized to show the input source impedance (R_{SOURCE}) between the 100 Ω to 10,000 Ω required to meet a 1-LSB settling at 12-bit, 10-bit, and 8-bit resolutions at different throughput in 1xREF (2.5 V) and 2xREF (5 V) input ranges.

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Typical Applications (continued)

9.2.2.2 Detailed Design Procedure

The design procedure is similar to the unbuffered-MXO application, but includes an operation amplifier in unity gain as a buffer. The most important parameter for multiplexer buffering is slew rate. The amplifier must finish slewing before the start of sampling (acquisition) to keep the buffer operating in small-signal mode during sampling (acquisition) time. Also, between the buffer output and converter input (INP), there must be a capacitor large enough to keep the buffer in small-signal operation during sampling (acquisition) time. Because 150 pF is large enough to protect the buffer form hold charge from internal capacitors, this value selected along with the lowest impedance that allows the op amp to remain stable.

The converter allows the MXO to settle approximately 600 ns before sampling. During this time, the buffer slews and then enters small-signal operation. For a 5-V step change, slew rate stays constant during the first 4 V. The last 1 V includes a transition from slewing and non-slewing. Thus, the buffer cannot be assumed to keep a constant slew during the 600 ns available for MXO settling. Assuming that the last 1-V slew is reduced to half is recommended. For this reason, slew is 10 V/µs or (5 V_{ref} + 1 V) / 0.6 µs to account for the 1-V slow slew. The OPA192 has a 20-V/us slew, and is capable of driving 150 pF with more than a 50° phase margin with a 50-Ω or 100-Ω R_{iso}, making the OPA192 an ideal selection for the ADS79xx-Q1 family of converters.

9.2.2.3 Application Curves

These curves show the R_{SOURCE} for an OPA192 buffered MXO.

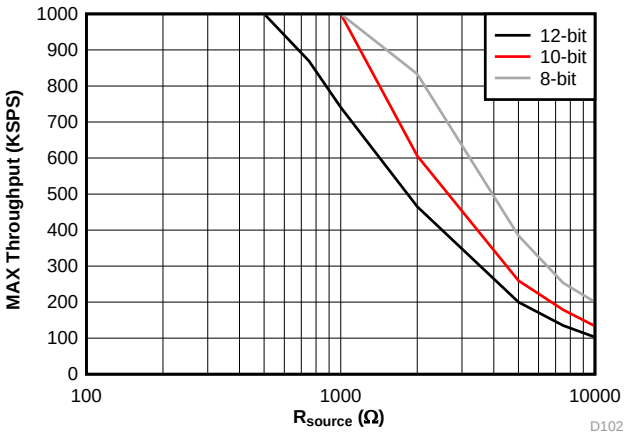

Figure 62. 2xREF Input Range Settling with an OPA192 MXO Buffer

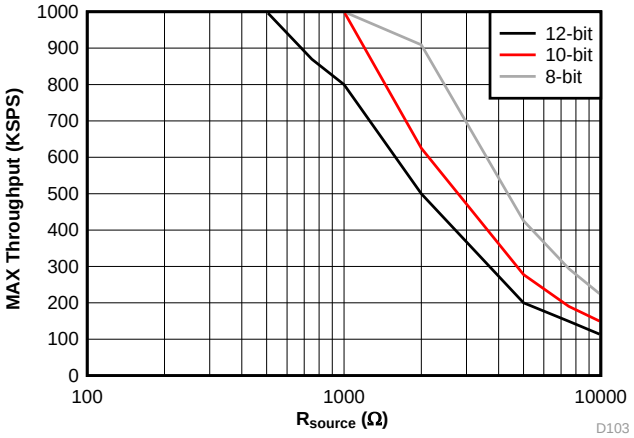

Figure 63. 1xREF Input Range Settling with an OPA192 MXO Buffer

9.3 Do's and Don'ts

- Use capacitors to decouple the dynamic current transients at each pins, including reference, supply, and input signal.
- Do not place capacitors on the MXO pin. This placement causes issues with the signal settling when the multiplexer changes channels.
- Depending on the PCB layout, there can be parasitic inductance on the SCLK trace that causes ringing. To minimize ringing, do not place a capacitor at the SCLK pin. Instead, place a small resistor in series with the SCLK pin to slow down the clock edges.

10 Power-Supply Recommendations

The devices are designed to operate from an analog supply voltage ($V_{(+VA)}$) range between 2.7 V and 5.25 V and a digital supply voltage ($V_{(+VBD)}$) range between 1.7 V and 5.25 V. Both supplies must be well regulated. The analog supply is always greater than or equal to the digital supply. A 1-µF ceramic decoupling capacitor is required at each supply pin and must be placed as close as possible to the device.

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11 Layout

11.1 Layout Guidelines

- A copper fill area underneath the device ties the AGND, BDGND, AINM, and REFM pins together. This copper fill area must also be connected to the analog ground plane of the PCB using at least four vias.
- The power sources must be clean and properly decoupled by placing a capacitor close to each of the three supply pins, as shown in Figure 64. To minimize ground inductance, ensure that each capacitor ground pin is connected to a grounding via by a very short and thick trace.
- The REFP pin requires a 10-µF ceramic capacitor to meet performance specifications. Place the capacitor directly next to the device. This capacitor ground pin must be routed to the REFM pin by a very short trace, as shown in Figure 64.
- Do not place any vias between a capacitor pin and a device pin.

NOTE

The full-power bandwidth of the converter makes the ADC sensitive to high frequencies in digital lines. Organize components in the PCB by keeping digital lines apart from the analog signal paths. This design configuration is critical to minimize crosstalk. For example, in Figure 64, input drivers are expected to be on the left of the converter and the microcontroller on the right.

11.2 Layout Example

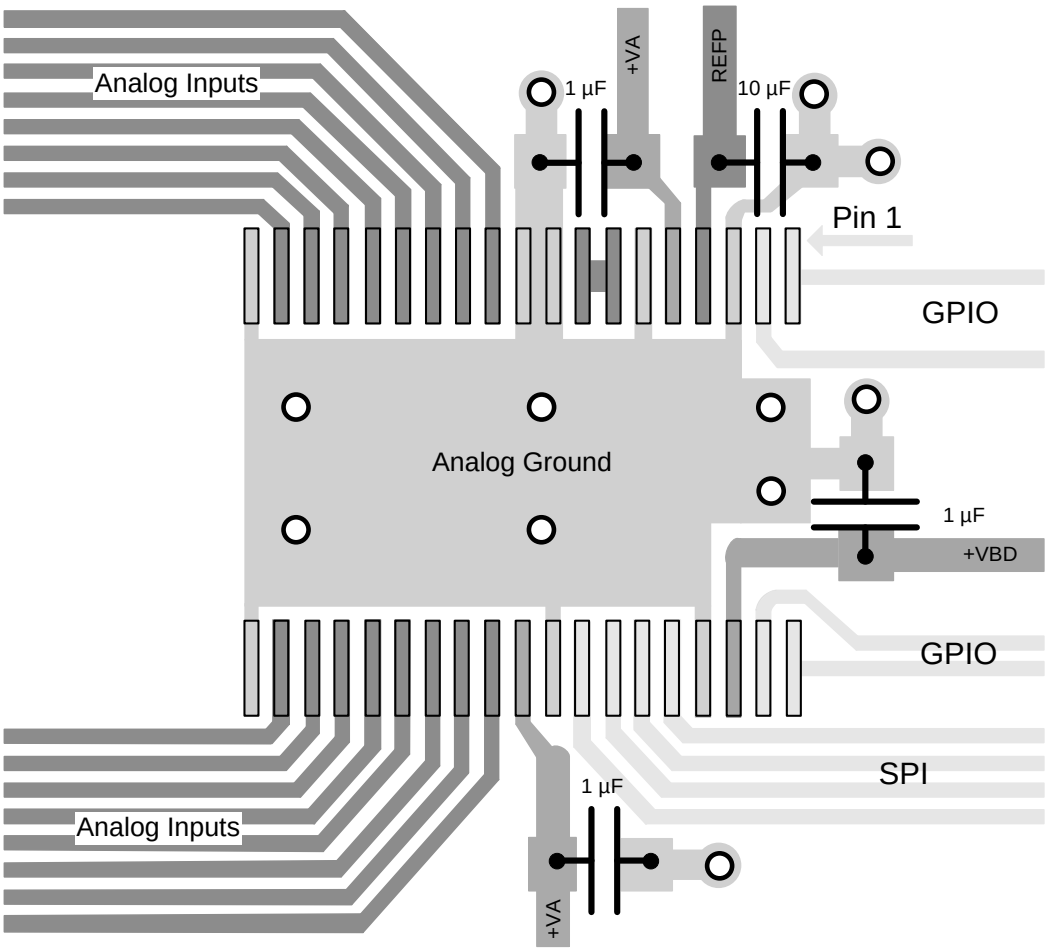

Figure 64. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- REF5025 Data Sheet, SBOS410
- OPA192 Data Sheet, SBOS620

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 14. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS7950-Q1	Click here	Click here	Click here	Click here	Click here
ADS7951-Q1	Click here	Click here	Click here	Click here	Click here
ADS7952-Q1	Click here	Click here	Click here	Click here	Click here
ADS7953-Q1	Click here	Click here	Click here	Click here	Click here
ADS7954-Q1	Click here	Click here	Click here	Click here	Click here
ADS7956-Q1	Click here	Click here	Click here	Click here	Click here
ADS7957-Q1	Click here	Click here	Click here	Click here	Click here
ADS7958-Q1	Click here	Click here	Click here	Click here	Click here
ADS7959-Q1	Click here	Click here	Click here	Click here	Click here
ADS7960-Q1	Click here	Click here	Click here	Click here	Click here
ADS7961-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

SPI is a trademark of Motorola Inc.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	O
ADS7950QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	
ADS7951QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	
ADS7952QDBTRQ1	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	
ADS7953QDBTRQ1	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	
ADS7954QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	
ADS7956QDBTRQ1	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	
ADS7957QDBTRQ1	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	
ADS7958QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	
ADS7959QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	
ADS7960QDBTRQ1	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	
ADS7961QDBTRQ1	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including t
do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in sp
reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm
flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a li
of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/B
lines if the finish value exceeds the maximum column width.

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provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate informatio
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis o
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF ADS7950-Q1, ADS7951-Q1, ADS7952-Q1, ADS7953-Q1, ADS7954-Q1, ADS7956-Q1, ADS7957-Q1, ADS7958-Q1, AD
Q1, ADS7961-Q1 :**

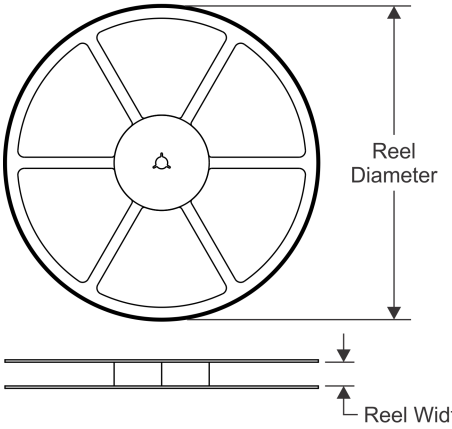
- Catalog: ADS7950, ADS7951, ADS7952, ADS7953, ADS7954, ADS7956, ADS7957, ADS7958, ADS7959, ADS7960, ADS7961

NOTE: Qualified Version Definitions:

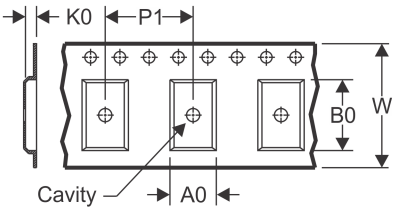
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

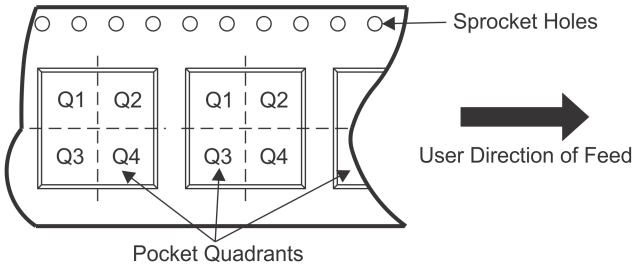


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

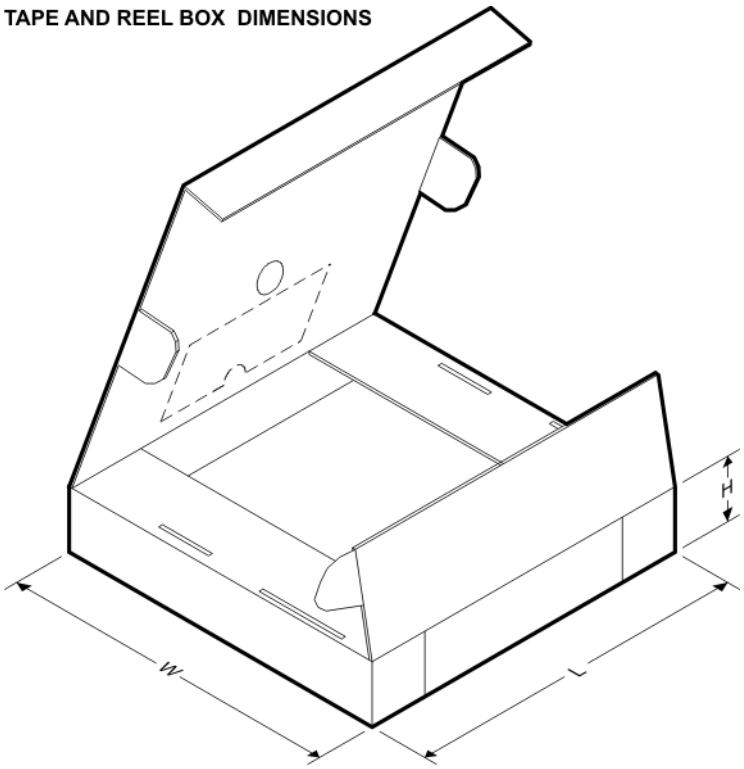
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7950QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7951QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7952QDBTRQ1	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7953QDBTRQ1	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7954QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7956QDBTRQ1	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7957QDBTRQ1	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7958QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7959QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7960QDBTRQ1	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7961QDBTRQ1	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

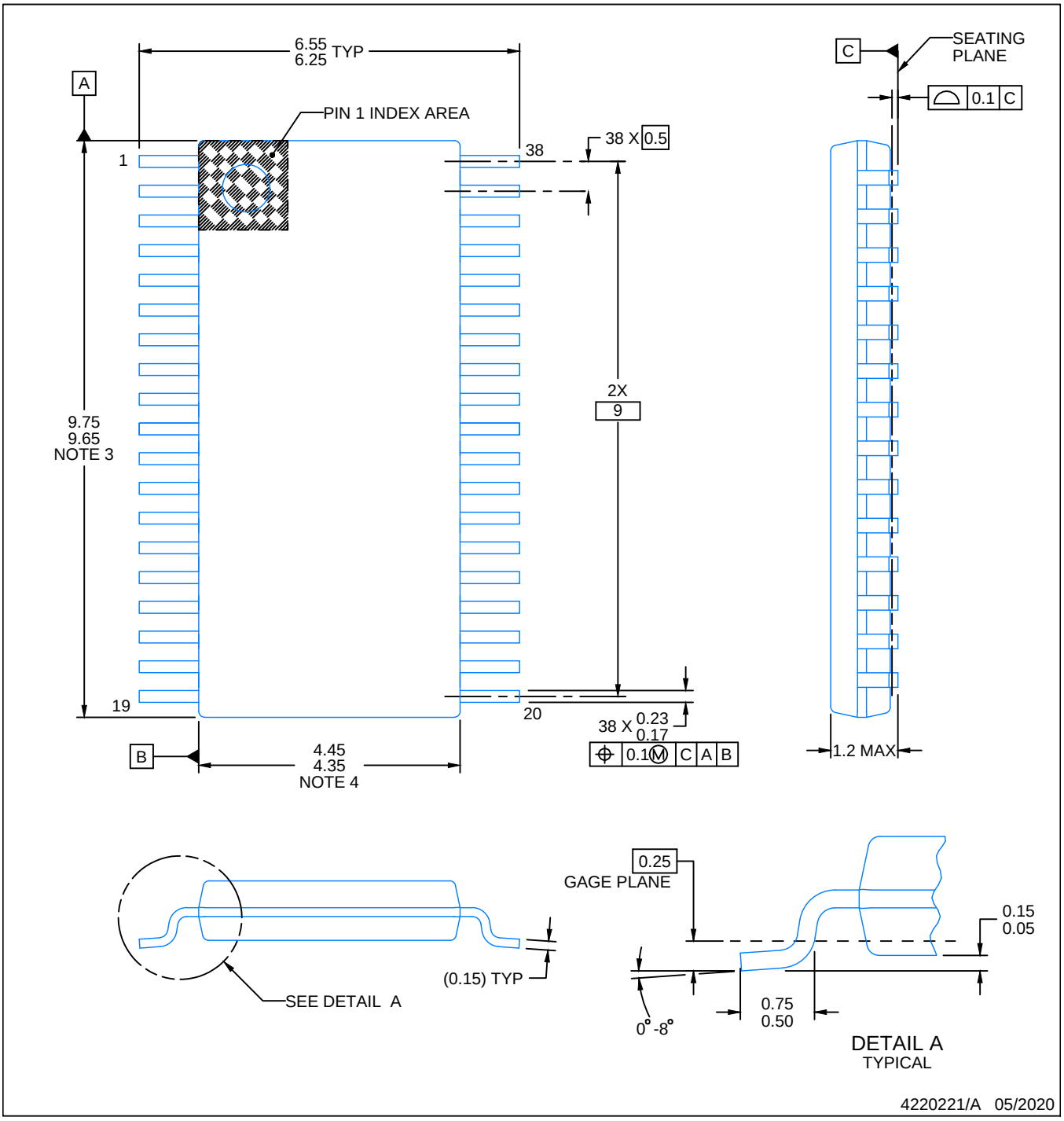
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7950QDBTRQ1	TSSOP	DBT	30	2000	853.0	449.0	35.0
ADS7951QDBTRQ1	TSSOP	DBT	30	2000	853.0	449.0	35.0
ADS7952QDBTRQ1	TSSOP	DBT	38	2000	853.0	449.0	35.0
ADS7953QDBTRQ1	TSSOP	DBT	38	2000	853.0	449.0	35.0
ADS7954QDBTRQ1	TSSOP	DBT	30	2000	853.0	449.0	35.0
ADS7956QDBTRQ1	TSSOP	DBT	38	2000	853.0	449.0	35.0
ADS7957QDBTRQ1	TSSOP	DBT	38	2000	853.0	449.0	35.0
ADS7958QDBTRQ1	TSSOP	DBT	30	2000	853.0	449.0	35.0
ADS7959QDBTRQ1	TSSOP	DBT	30	2000	853.0	449.0	35.0
ADS7960QDBTRQ1	TSSOP	DBT	38	2000	853.0	449.0	35.0
ADS7961QDBTRQ1	TSSOP	DBT	38	2000	853.0	449.0	35.0

PACKAGE OUTLINE

DBT0038A

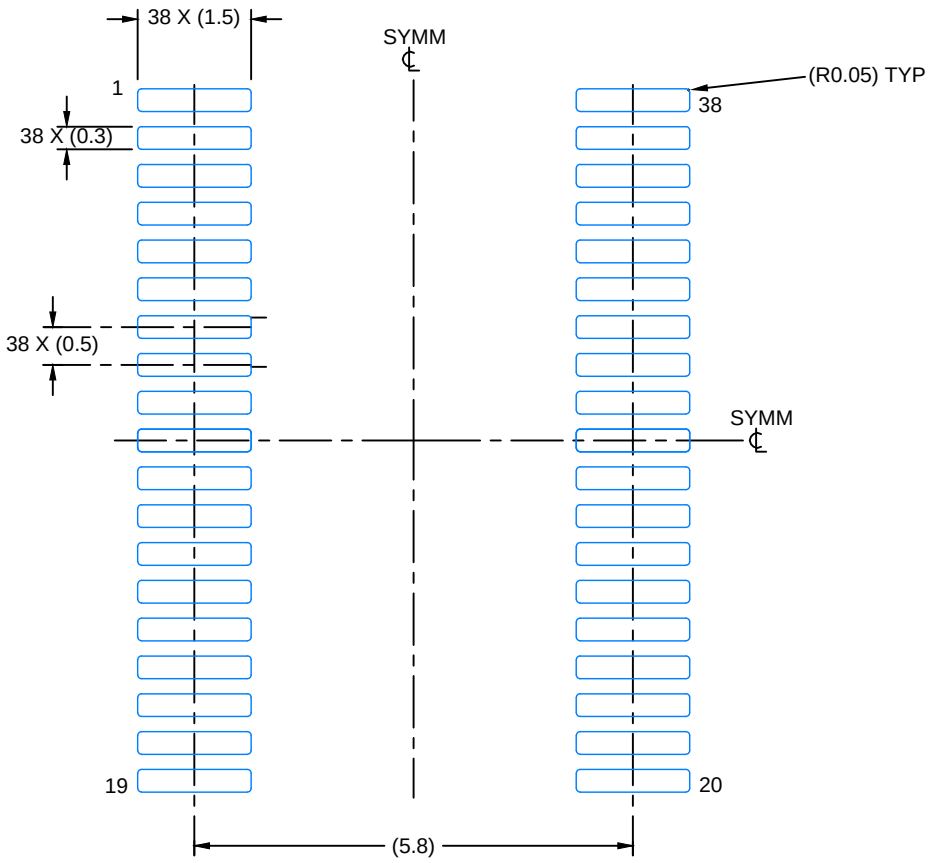
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

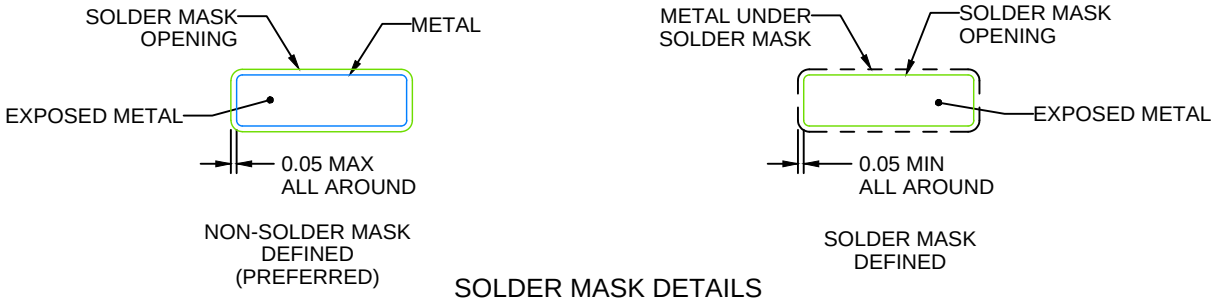


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

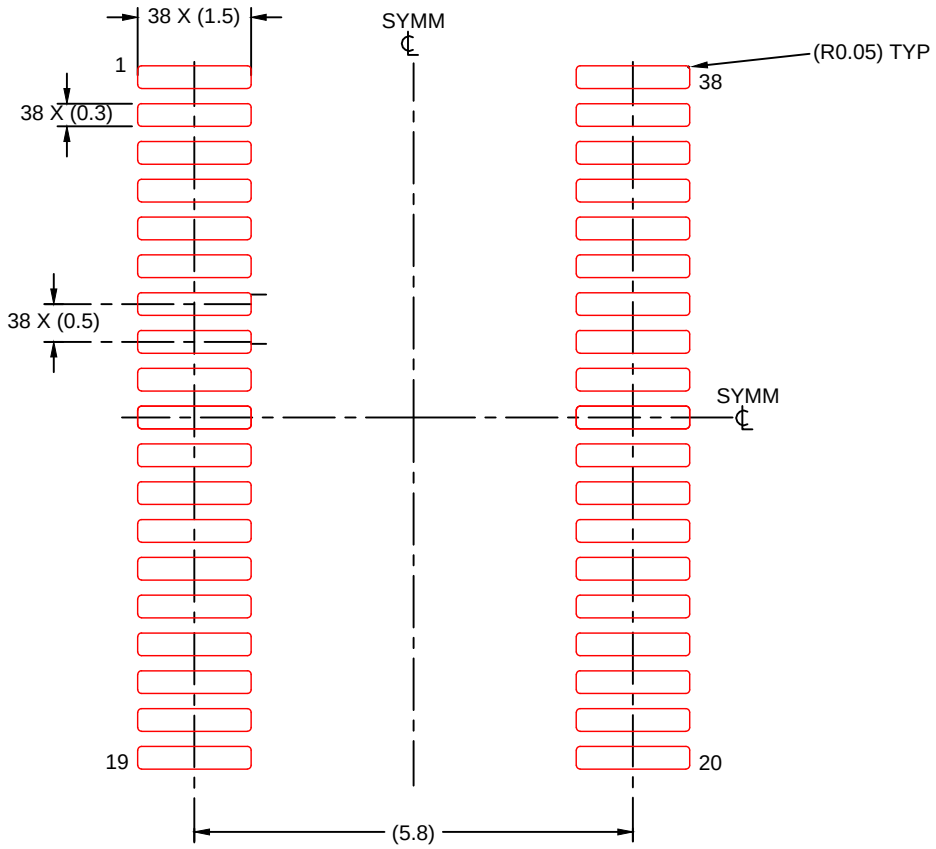


SOLDER MASK DETAILS

4220221/A 05/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220221/A 05/2020

NOTES: (continued)

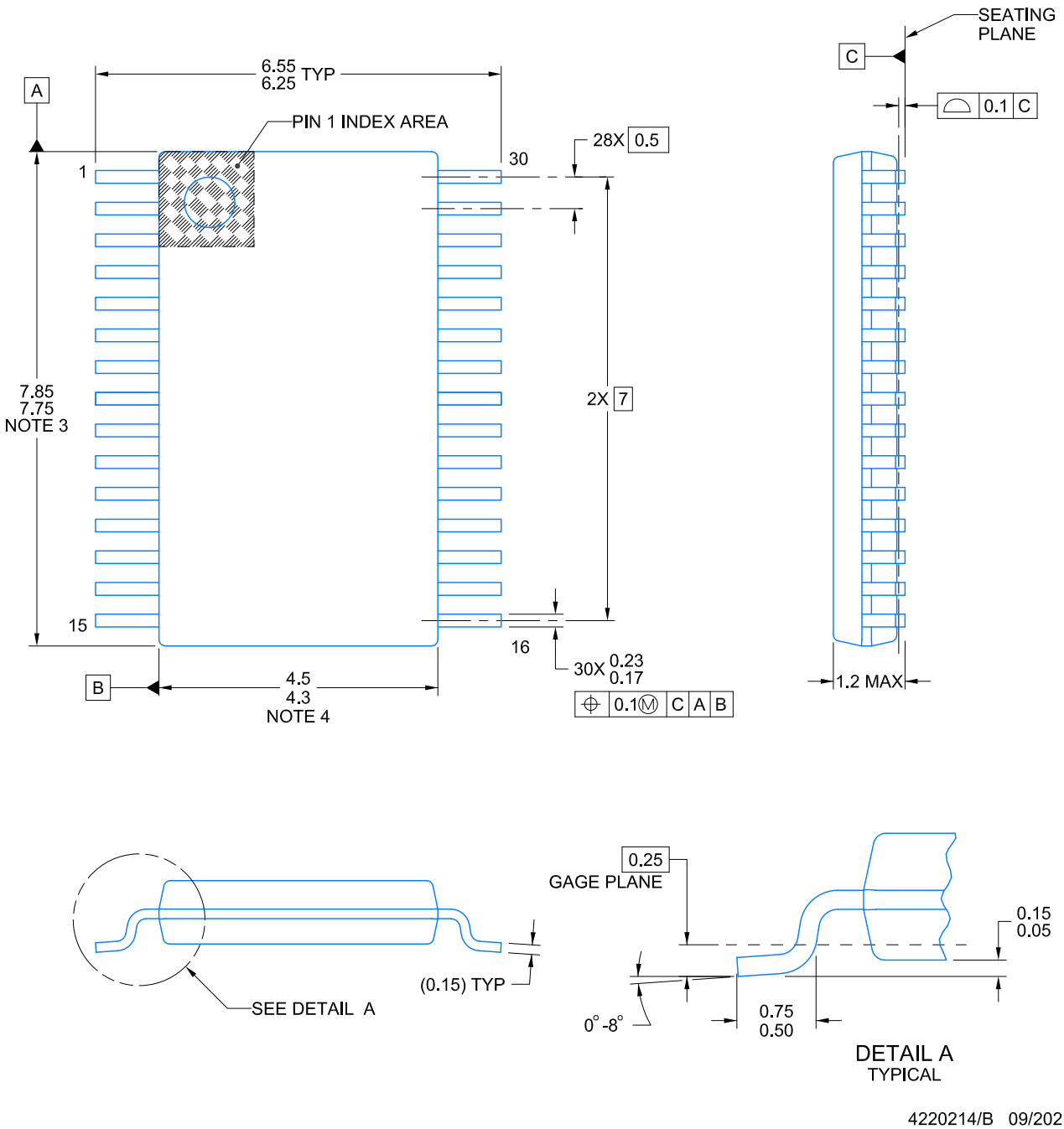
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBT0030A

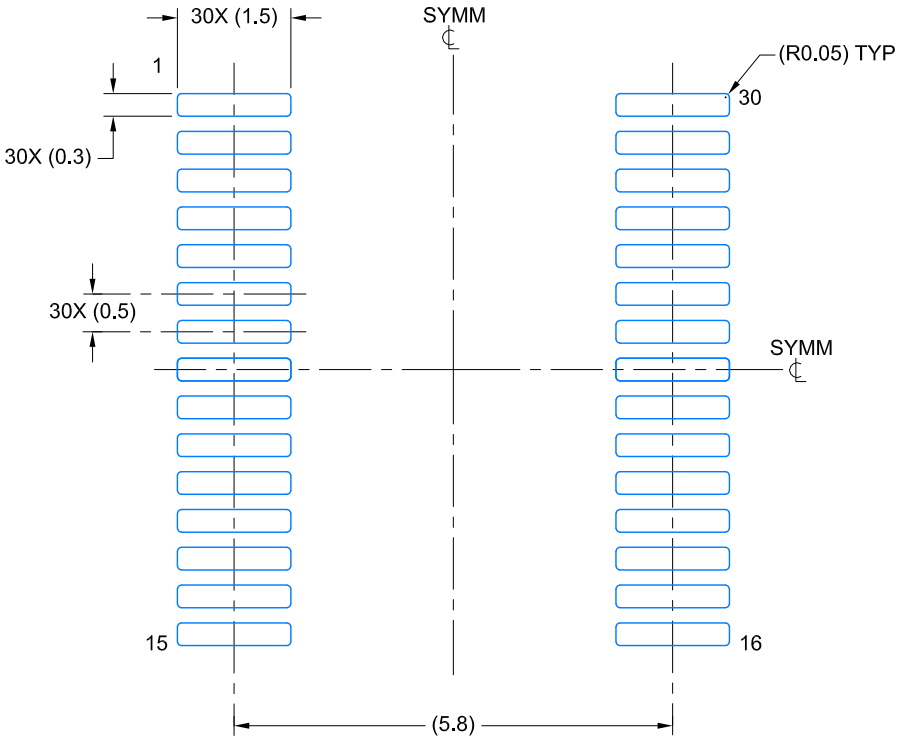
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

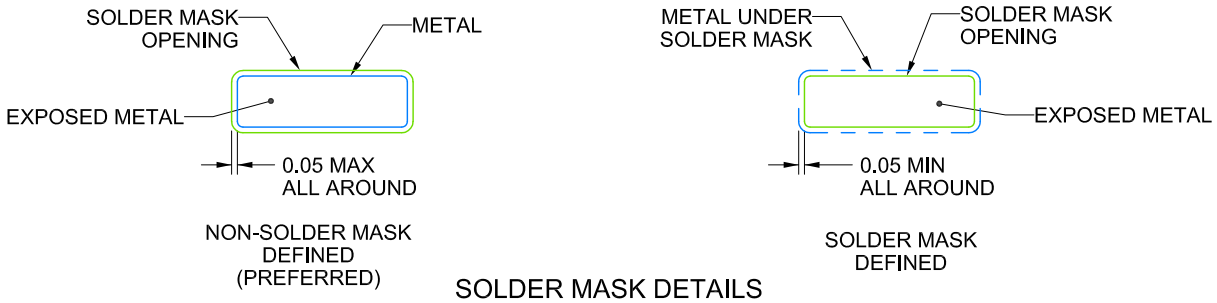


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

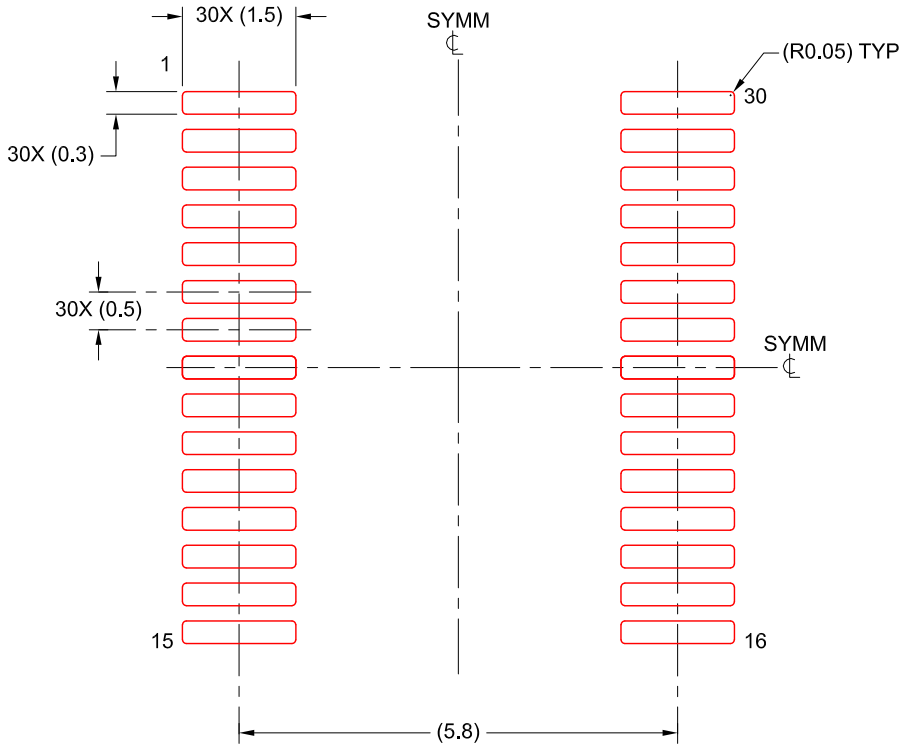


SOLDER MASK DETAILS

4220214/B 09/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220214/B 09/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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