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# CSD17575Q3T

Texas instruments

MOSFET 30V,NCh NexFET Pwr MOSFET

Any questions,please feel free to contact us.  
[info@kaimte.com](mailto:info@kaimte.com)

# CSD17575Q3 30-V N-Channel NexFET™ Power MOSFET

## 1 Features

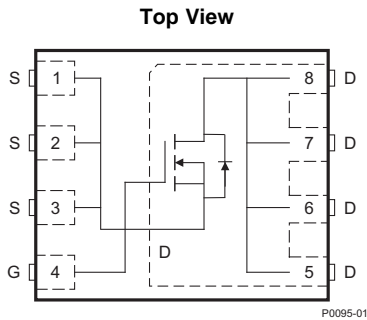
- Low  $Q_g$  and  $Q_{gd}$
- Low  $R_{DS(on)}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3 mm x 3.3 mm Plastic Package

## 2 Applications

- Point of Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Synchronous FET Applications

## 3 Description

This 1.9 mΩ, 30 V, SON 3x3 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	30	V
$Q_g$	Gate Charge Total (4.5V)	23	nC
$Q_{gd}$	Gate Charge Gate-to-Drain	5.4	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	2.6
		$V_{GS} = 10\text{ V}$	1.9
$V_{th}$	Threshold Voltage	1.4	V

### Ordering Information<sup>(1)</sup>

Device	Media	Qty	Package	Ship
CSD17575Q3	13-Inch Reel	2500	SON 3.3 x 3.3 mm Plastic Package	Tape and Reel
CSD17575Q3T	13-Inch Reel	250		

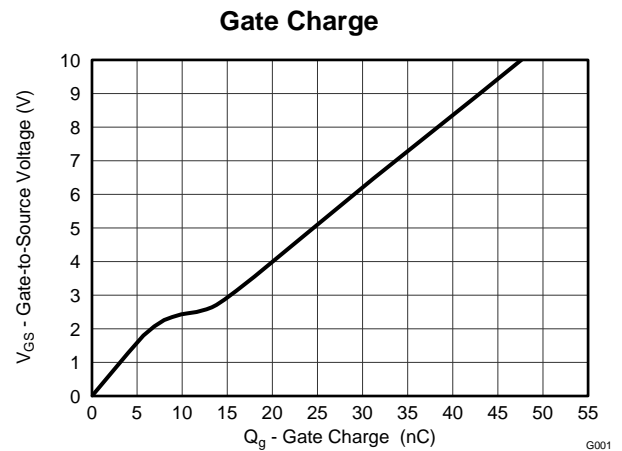
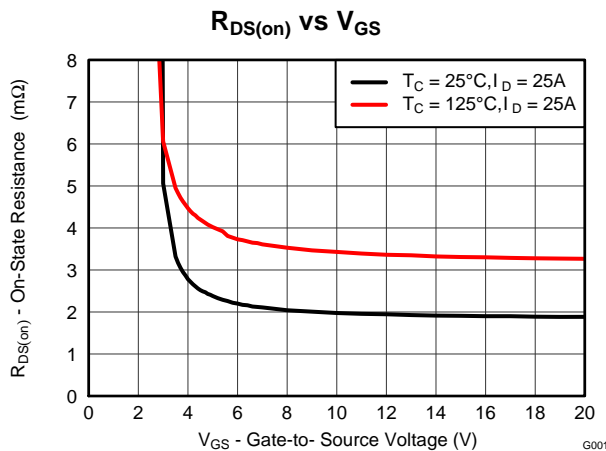
(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current (Package Limit)	60	A
	Continuous Drain Current (Silicon Limit), $T_C = 25^\circ\text{C}$	182	
	Continuous Drain Current <sup>(1)</sup>	27	
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	240	A
$P_D$	Power Dissipation <sup>(1)</sup>	2.8	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	108	
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 48, L = 0.1\text{ mH}, R_G = 25\ \Omega$	115	mJ

(1) Typical  $R_{\theta JA} = 45^\circ\text{C/W}$  on 1-inch<sup>2</sup> Cu (2 oz.) on 0.060-inch thick FR4 PCB.

(2) Max  $R_{\theta JC} = 1.5^\circ\text{C/W}$ , pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$



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## 4 Revision History

### Changes from Original (June 2014) to Revision A

**Page**

<ul style="list-style-type: none"> <li>• Added b1, d, d1, and K dimensions to the mechanical information table ..... 8</li> </ul>	<b>8</b>
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## 5 Specifications

### 5.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

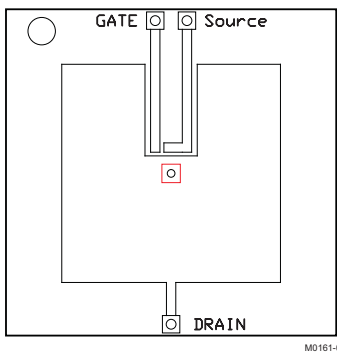
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.1	1.4	1.8	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$		2.6	3.2	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$		1.9	2.3	
$g_{fs}$	Transconductance	$V_{DS} = 3\text{ V}, I_D = 25\text{ A}$		118		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		3400	4420	pF
$C_{OSS}$	Output Capacitance			393	511	pF
$C_{RSS}$	Reverse Transfer Capacitance			157	204	pF
$R_g$	Series Gate Resistance	$V_{DS} = 15\text{ V}, I_D = 25\text{ A}$		0.9	1.8	$\Omega$
$Q_g$	Gate Charge Total (4.5 V)			23	30	nC
$Q_{gd}$	Gate Charge Gate-to-Drain			5.4		nC
$Q_{gs}$	Gate Charge Gate-to-Source			8.5		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			4.6		nC
$Q_{OSS}$	Output Charge	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$		11.6		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$ $R_G = 2\ \Omega$		4		ns
$t_r$	Rise Time			10		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
$t_f$	Fall Time			3		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode Forward Voltage	$I_S = 25\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 15\text{ V}, I_F = 25\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		15		nC
$t_{rr}$	Reverse Recovery Time			13		ns

### 5.2 Thermal Information

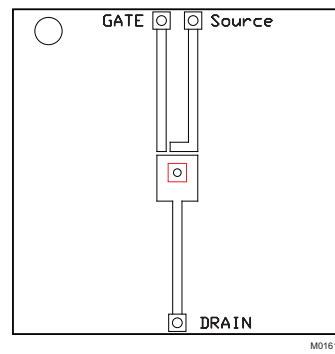
( $T_A = 25^\circ\text{C}$  unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance <sup>(1)</sup>			1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>(1)(2)</sup>			55	

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), Cu pad on a 1.5-inches x 1.5-inches thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> 2-oz.Cu.



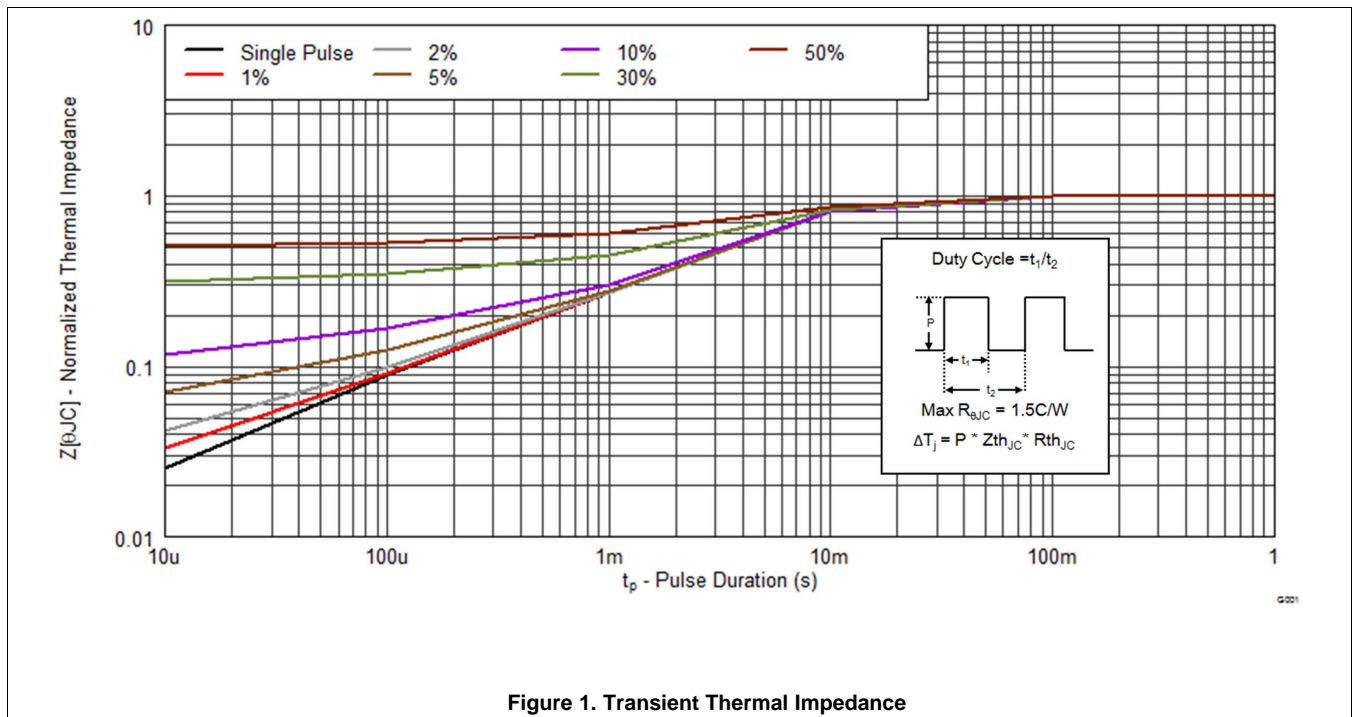
Max  $R_{\theta JA} = 55^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> of 2 oz. Cu.



Max  $R_{\theta JA} = 160^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of  
2 oz. Cu.

### 5.3 Typical MOSFET Characteristics

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

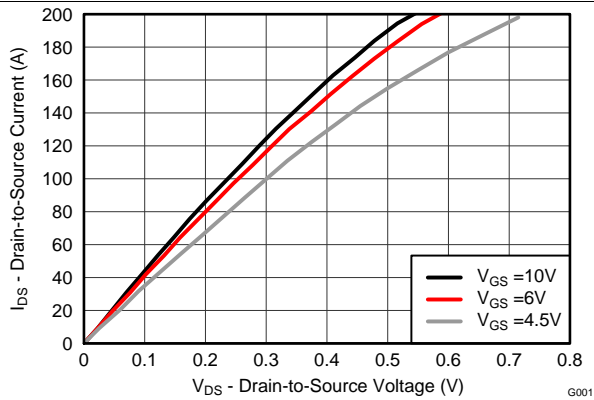


Figure 2. Saturation Characteristics

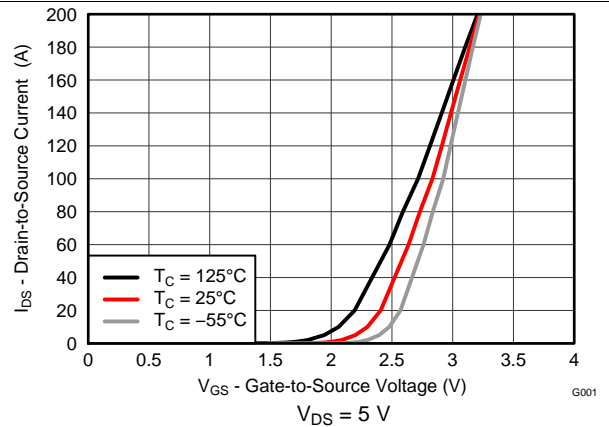


Figure 3. Transfer Characteristics

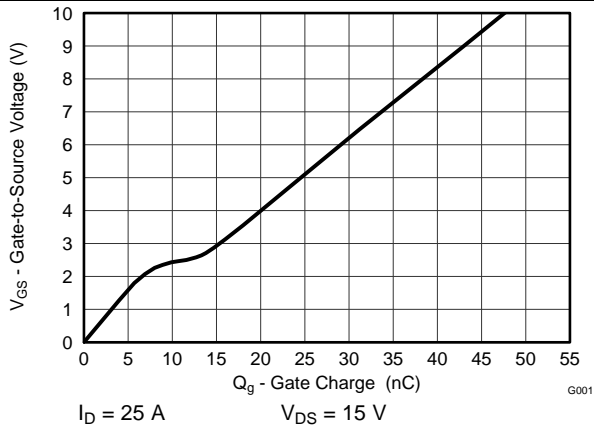


Figure 4. Gate Charge

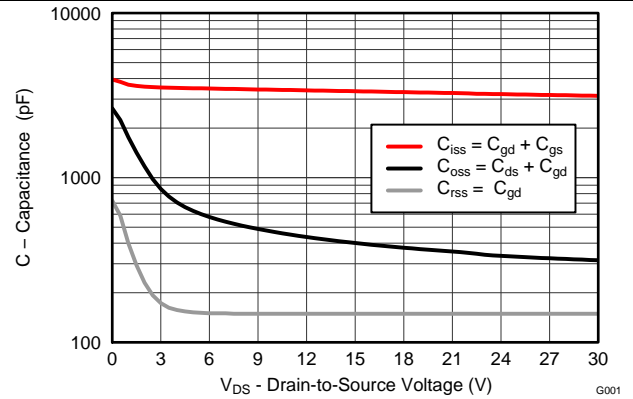


Figure 5. Capacitance

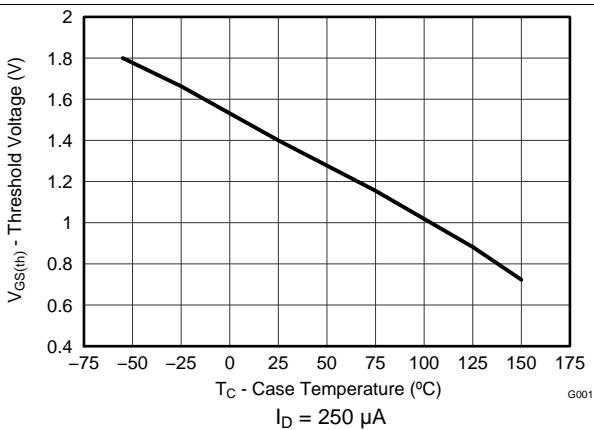


Figure 6. Threshold Voltage vs Temperature

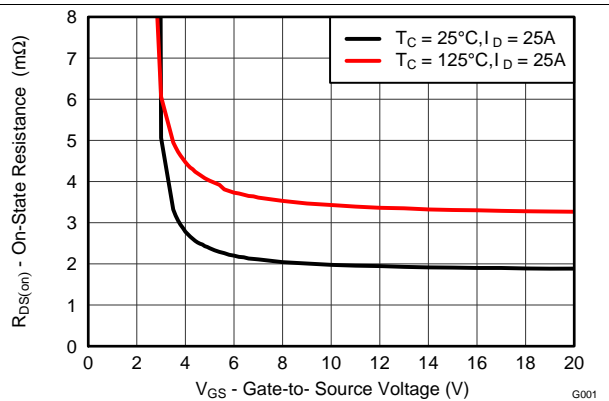


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

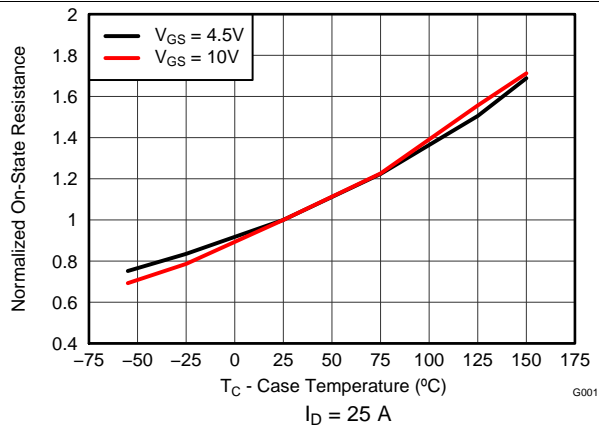


Figure 8. Normalized On-State Resistance vs Temperature

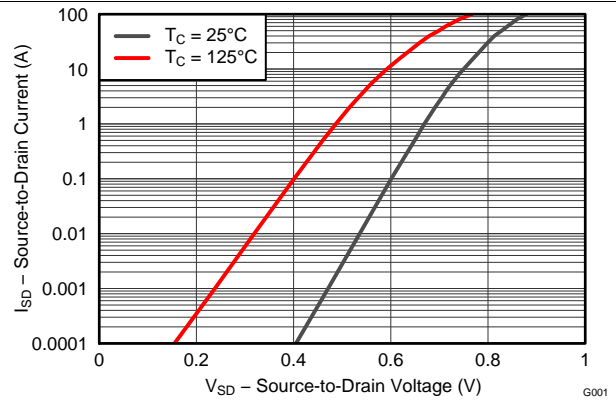


Figure 9. Typical Diode Forward Voltage

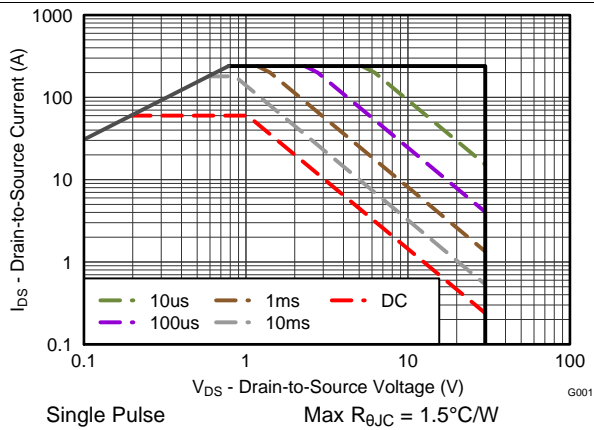


Figure 10. Maximum Safe Operating Area

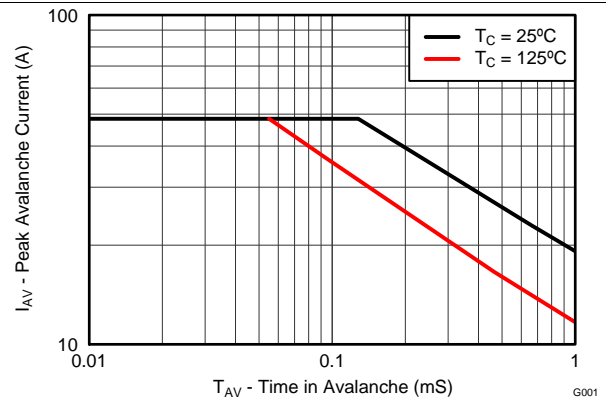


Figure 11. Single Pulse Unclamped Inductive Switching

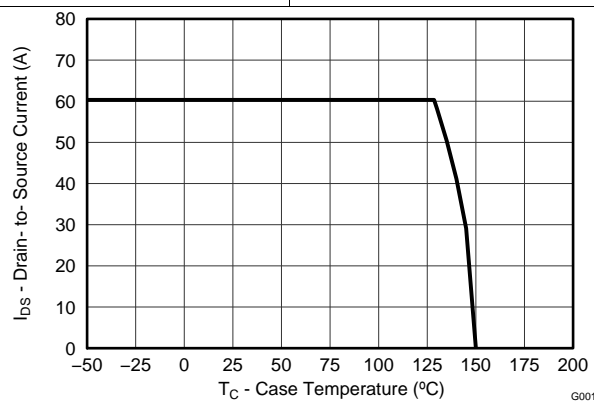


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Trademarks

NexFET is a trademark of Texas Instruments.

### 6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.3 Glossary

[SLYZ022](#) — *TI Glossary*.

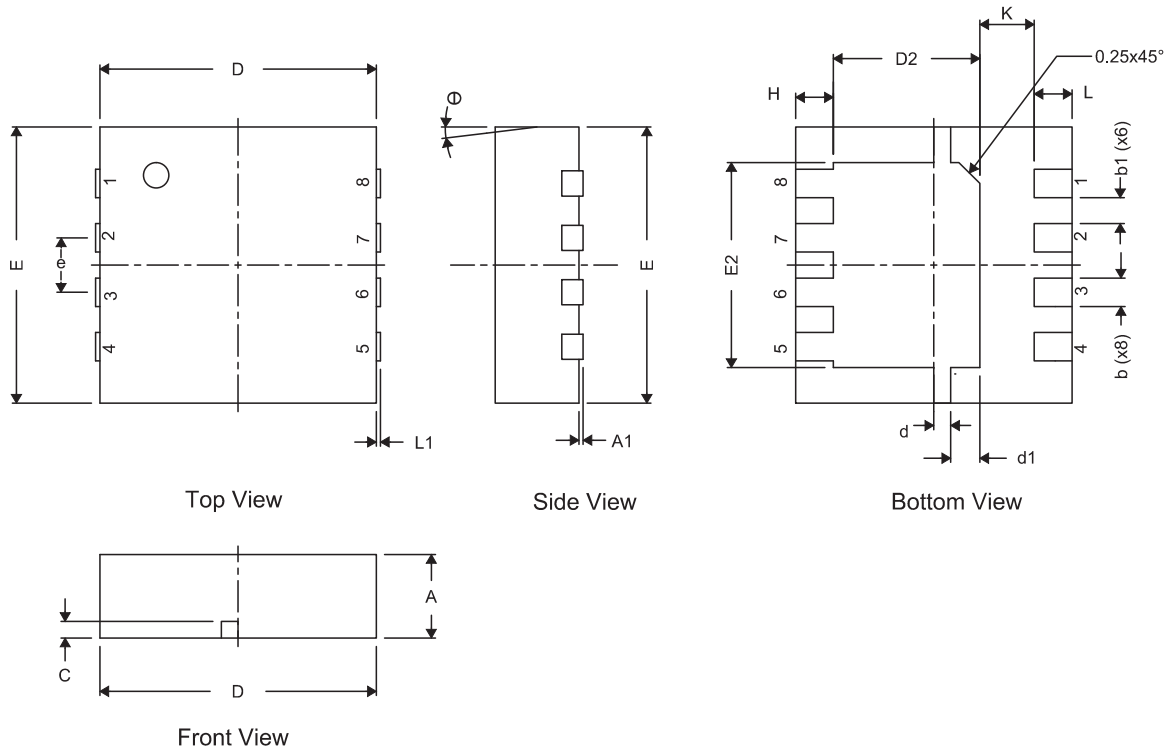
This glossary lists and explains terms, acronyms, and definitions.



## 7 Mechanical, Packaging, and Orderable Information

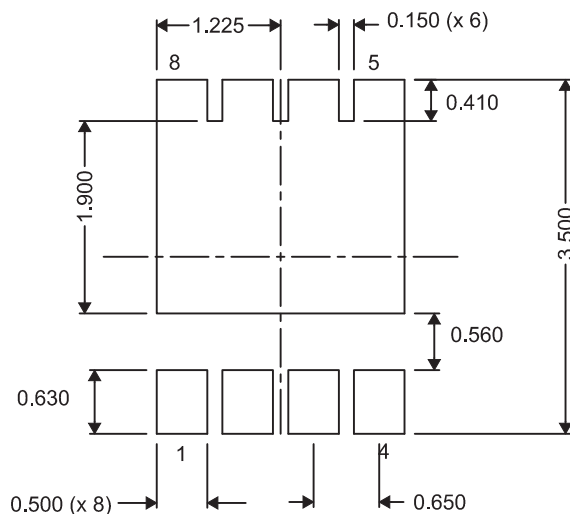
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Q3 Package Dimensions



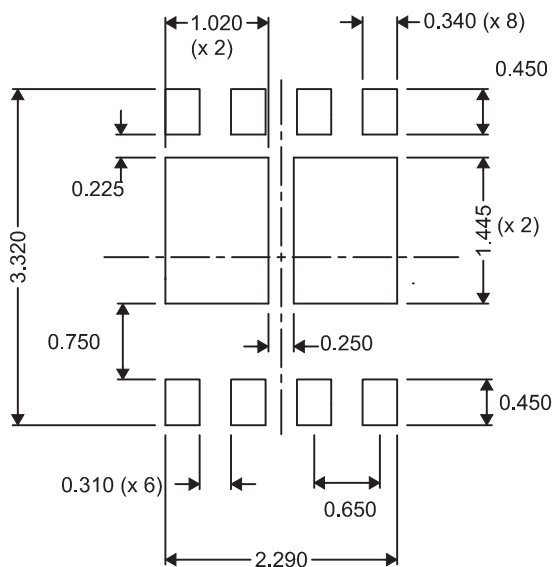
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
$\theta$	0	—	0	0	—	0

### 7.2 Recommended PCB Pattern



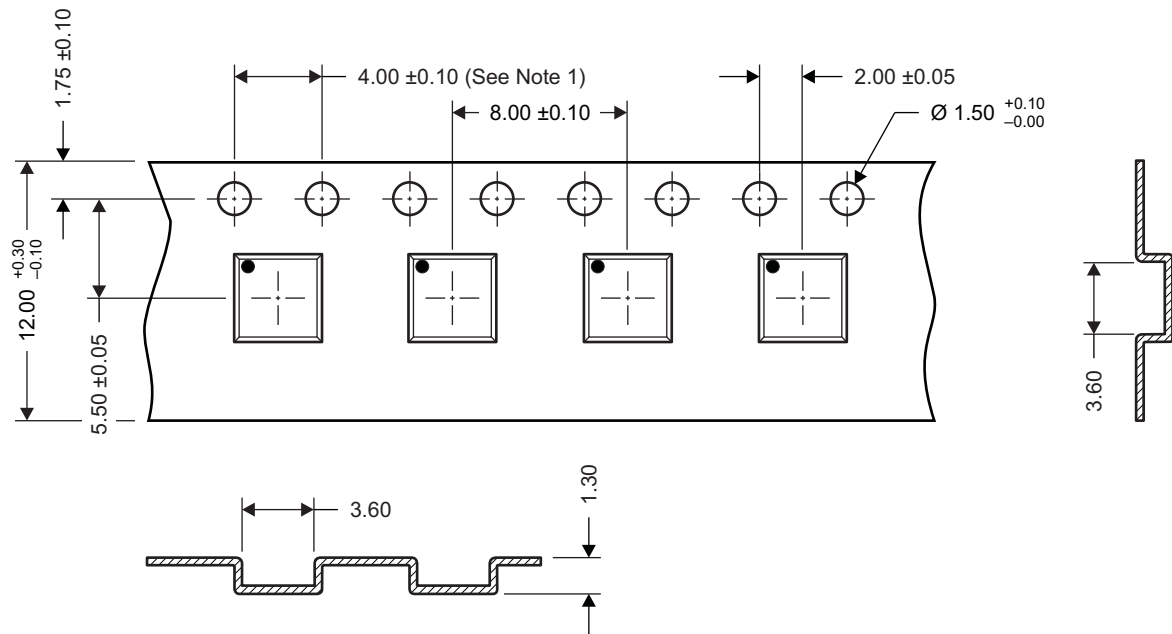
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

### 7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

## 7.4 Q3 Tape and Reel Information



M0144-01

### Notes:

- 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
- Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
- Material: black static dissipative polystyrene
- All dimensions are in mm (unless otherwise specified).
- Thickness:  $0.30 \pm 0.05$  mm
- MSL1 260°C (IR and Convection) PbF Reflow Compatible

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	O
CSD17575Q3	ACTIVE	VSON-CLIP	DQG	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	
CSD17575Q3T	ACTIVE	VSON-CLIP	DQG	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including but not limited to lead (Pb). All RoHS substances must not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in applications that reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm. All other flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line item is followed by a device marking in parentheses, it represents the device marking for that device. If a line item is followed by two device markings in parentheses, the first marking represents the device marking for that device and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values are limited to a maximum of 100 characters. Values exceeding this limit will be truncated. Lead finish/Ball material values are limited to a maximum of 100 characters. Values exceeding this limit will be truncated. Lead finish/Ball material values are limited to a maximum of 100 characters. Values exceeding this limit will be truncated.

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