



# STD60NF55LA

N-channel 55 V, 0.012  $\Omega$ , 60 A DPAK  
STripFET™ II Power MOSFET

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD60NF55LA	55V	<0.015 $\Omega$	60A

- Low threshold drive

## Applications

- Switching application
- Automotive

## Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

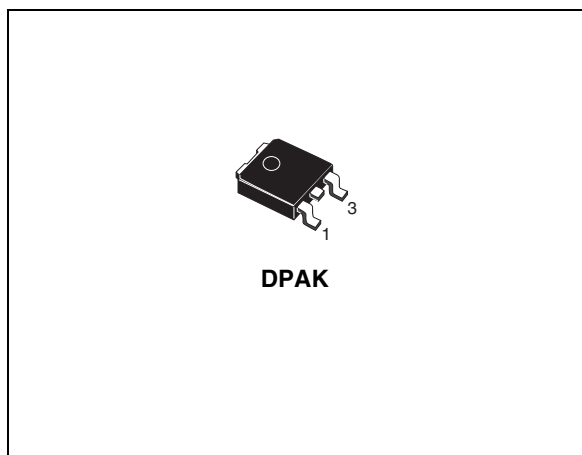


Figure 1. Internal schematic diagram

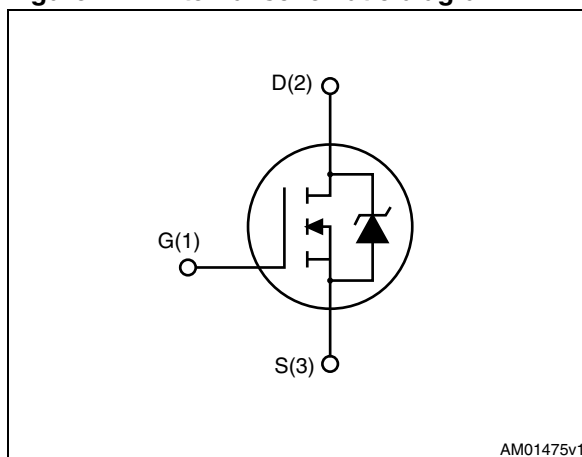


Table 1. Device summary

Order code	Marking	Package	Packaging
STD60NF55LA	D60NF55LA	DPAK	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	55	V
$V_{GS}$	Gate- source voltage	$\pm 15$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	60	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	42	A
$I_{DM}^{(1)}$	Drain current (pulsed)	240	A
$P_{tot}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
	Derating factor	0.73	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	16	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	400	mJ
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 40\text{ A}$ ,  $di/dt \leq 350\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .
3. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 17.5\text{ A}$ ,  $V_{DD} = 24\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.36	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-to ambient max	100	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0$	55			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 55 \text{ V}$ $V_{DS} = 55 \text{ V}$ , $T_C = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 15 \text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	1		2	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 30 \text{ A}$ $V_{GS} = 5 \text{ V}$ , $I_D = 30 \text{ A}$		0.012 0.014	0.015 0.017	$\Omega$ $\Omega$
$I_{D(on)}$	On state drain current	$V_{GS} = 3.5 \text{ V}$ , $V_{DS} \geq 12 \text{ V}$ $-55^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$	35			A

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10 \text{ V}$ , $I_D = 30 \text{ A}$	-	35		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$	-	1950 390 130		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 25 \text{ V}$ , $I_D = 30 \text{ A}$ $R_G = 4.7 \Omega$ , $V_{GS} = 4.5 \text{ V}$ (see <a href="#">Figure 14</a> )	-	30 180 80 35		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 40 \text{ V}$ , $I_D = 60 \text{ A}$ , $V_{GS} = 5 \text{ V}$ , $R_G = 4.7 \Omega$ (see <a href="#">Figure 15</a> )	-	40 10 20	56	nC nC nC

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		60 240	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 60\text{ A}$ , $V_{GS} = 0$	-		1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 40\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 25\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	65 130 4		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

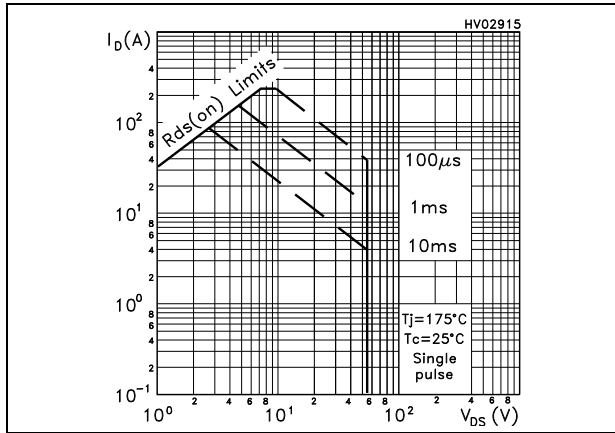


Figure 3. Thermal impedance

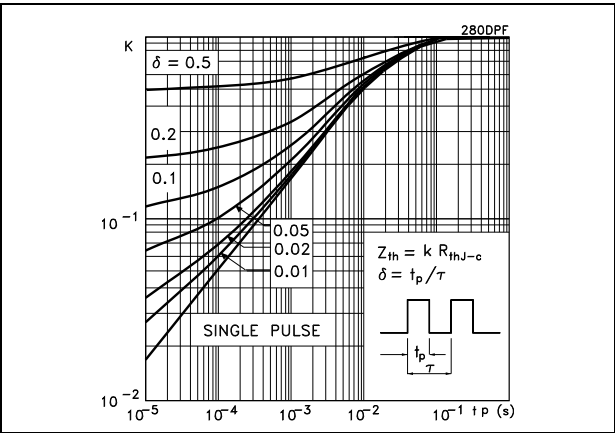


Figure 4. Output characteristics

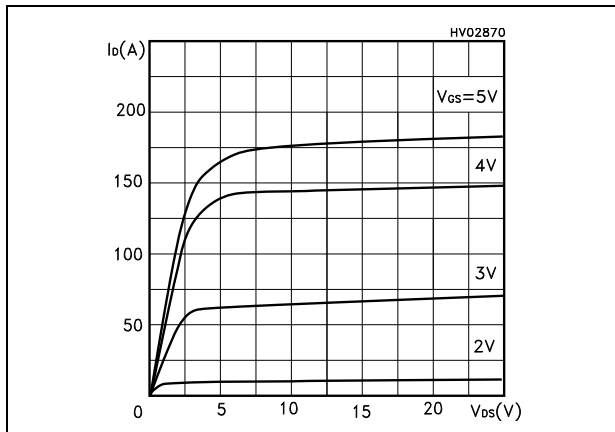


Figure 5. Transfer characteristics

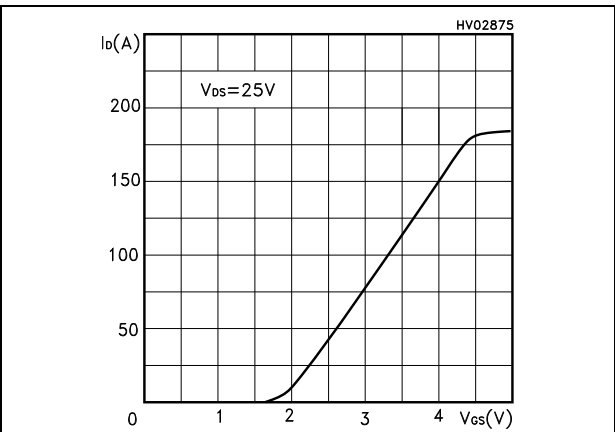


Figure 6. Transconductance

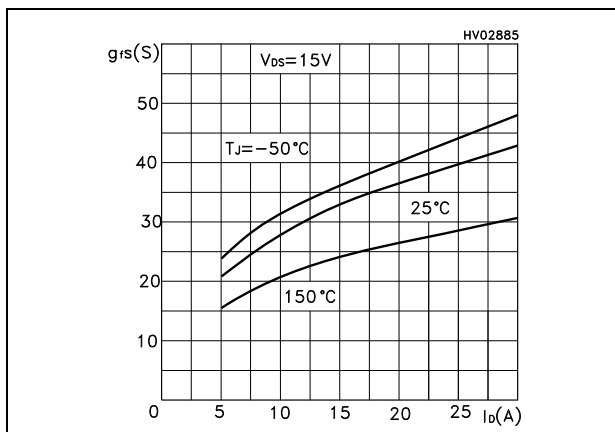


Figure 7. Static drain-source on resistance

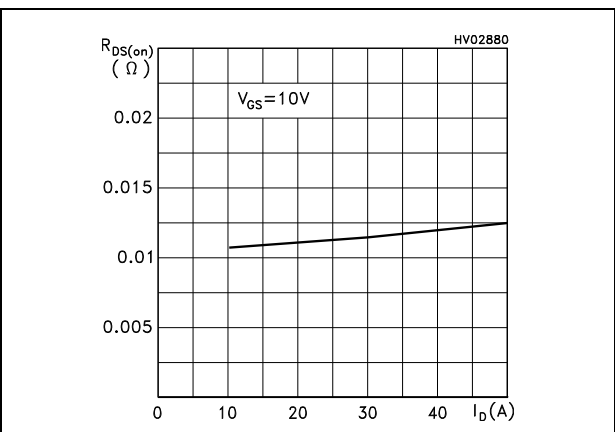


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

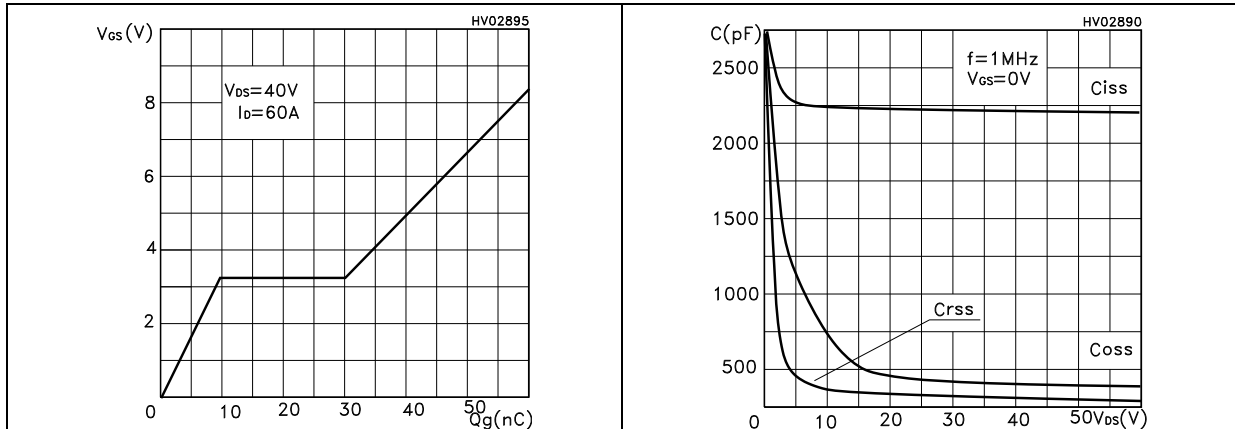


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

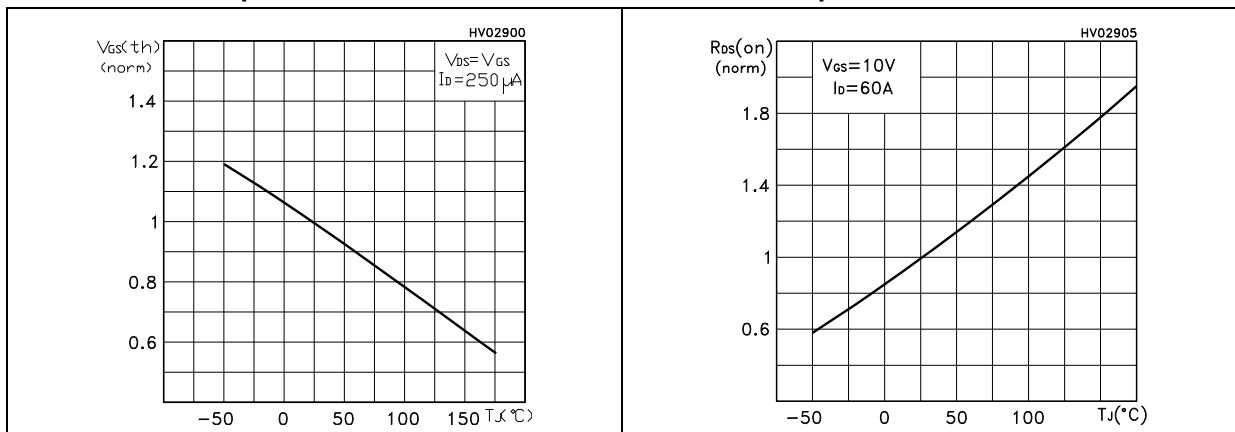


Figure 12. Source-drain diode forward characteristics

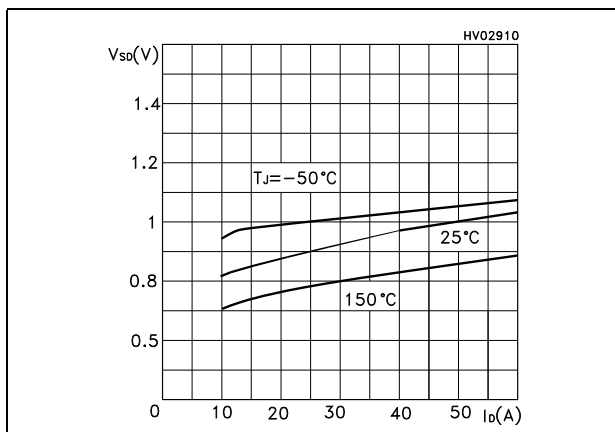
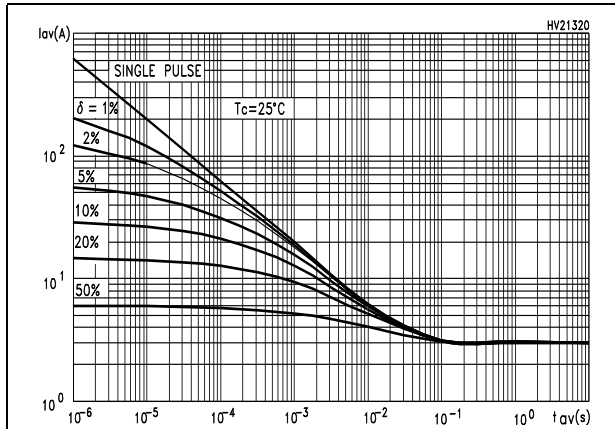


Figure 13. Allowable  $I_{AV}$  vs time in avalanche



The previous curve gives the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$$P_{D(AVE)} = 0.5 * (1.3 * BV_{DSS} * I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$$

Where:

$I_{AV}$  is the allowable current in avalanche,

$P_{D(AVE)}$  is the average power dissipation in avalanche (single pulse)

$t_{AV}$  is the time in avalanche.

To derate above 25°C, at fixed  $I_{AV}$ , the following equation must be applied:

$$I_{AV} = 2 * (T_{jmax} - T_{CASE}) / (1.3 * BV_{DSS} * Z_{th})$$

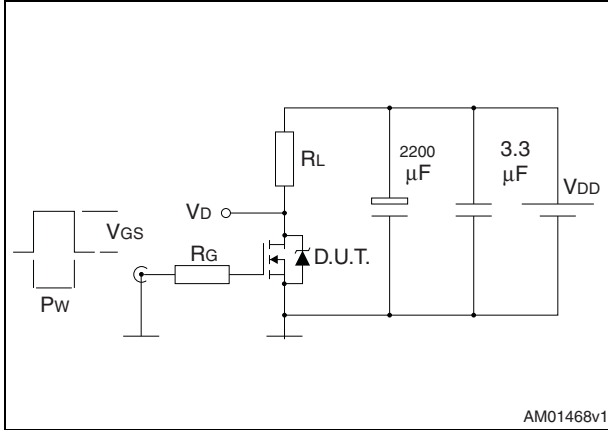
Where:

$Z_{th} = K * R_{th}$  is the value coming from normalized thermal response at fixed pulse width equal to  $T_{AV}$



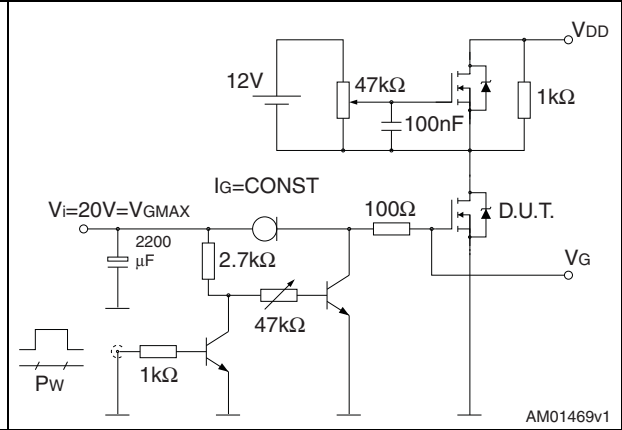
### 3 Test circuit

**Figure 14. Switching times test circuit for resistive load**



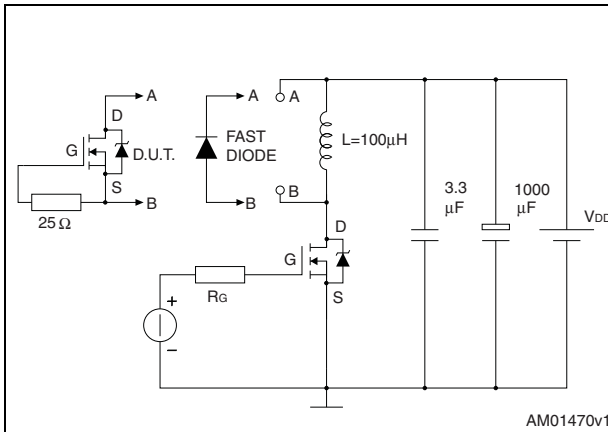
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**Figure 15. Gate charge test circuit**



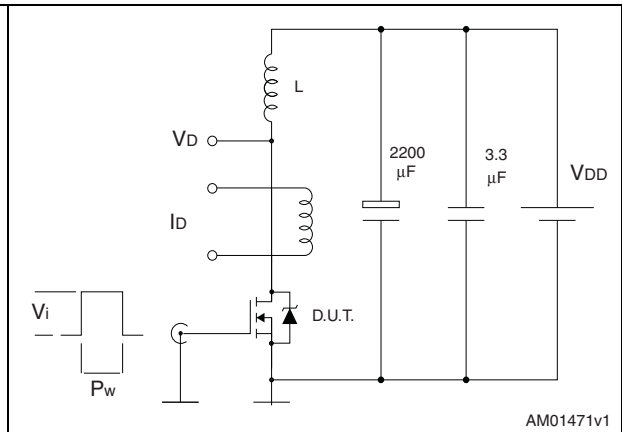
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**Figure 16. Test circuit for inductive load switching and diode recovery times**



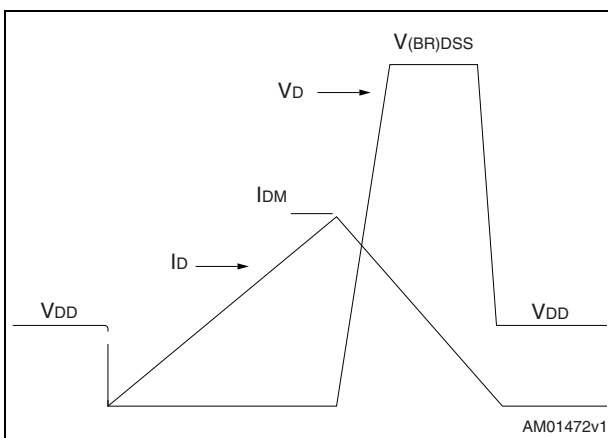
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**Figure 17. Unclamped Inductive load test circuit**



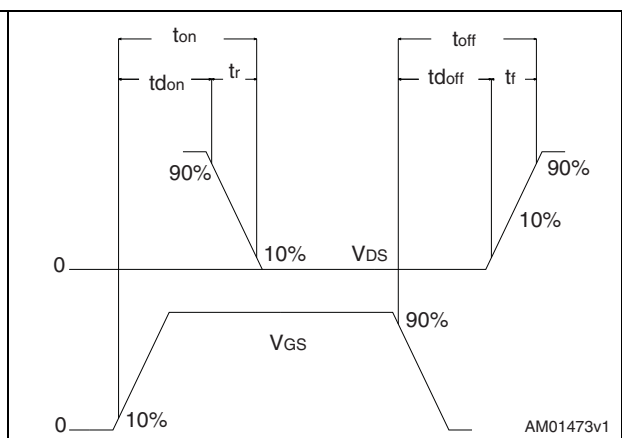
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**Figure 18. Unclamped inductive waveform**



AM01472v1

**Figure 19. Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 7. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) drawing

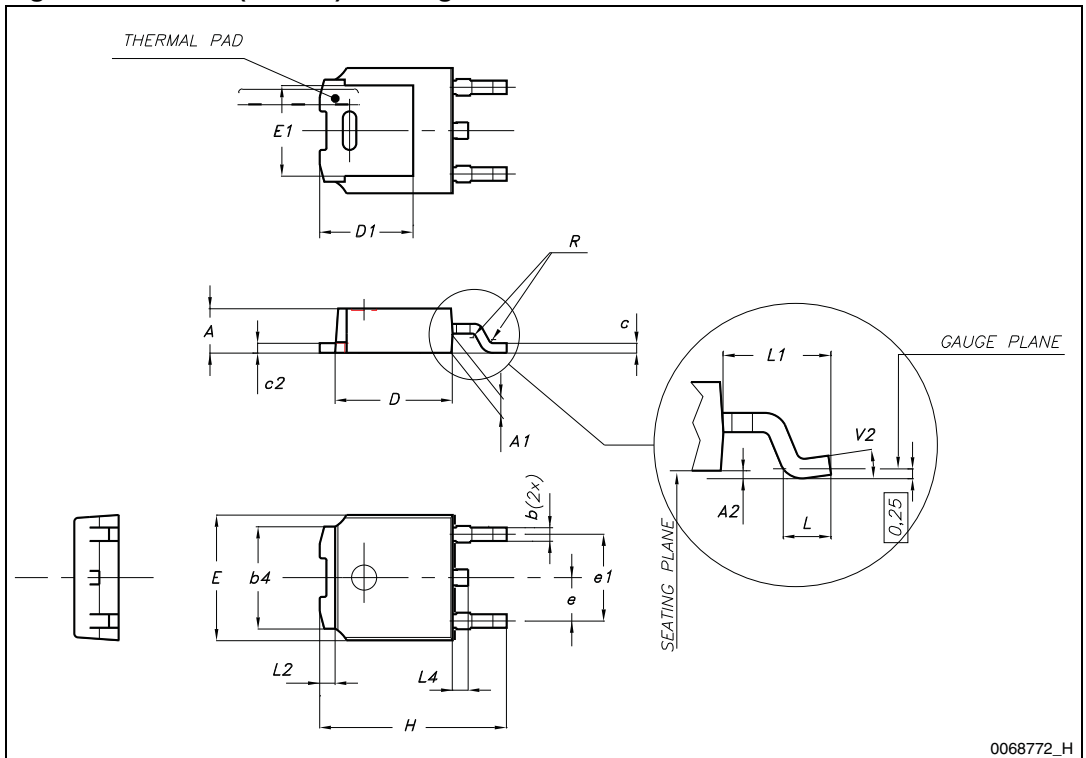
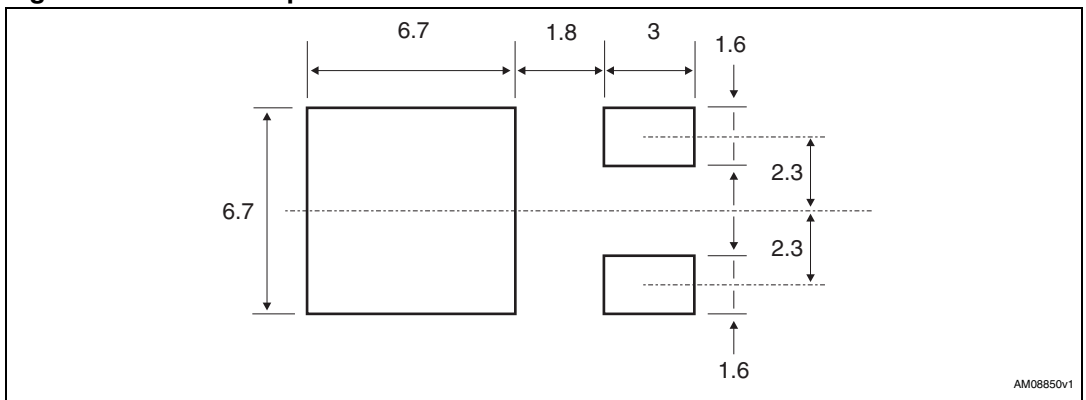


Figure 21. DPAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

## 5 Packing mechanical data

Table 8. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 22. Tape for DPAK (TO-252)

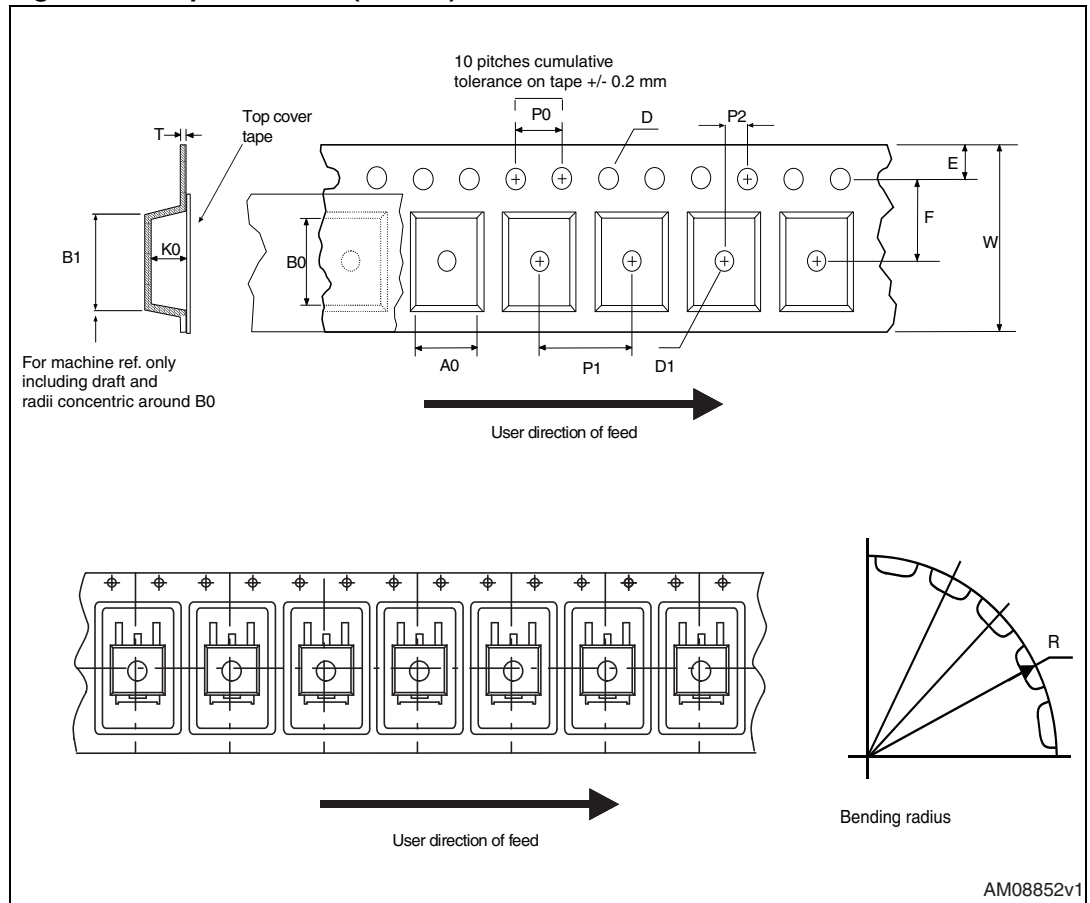
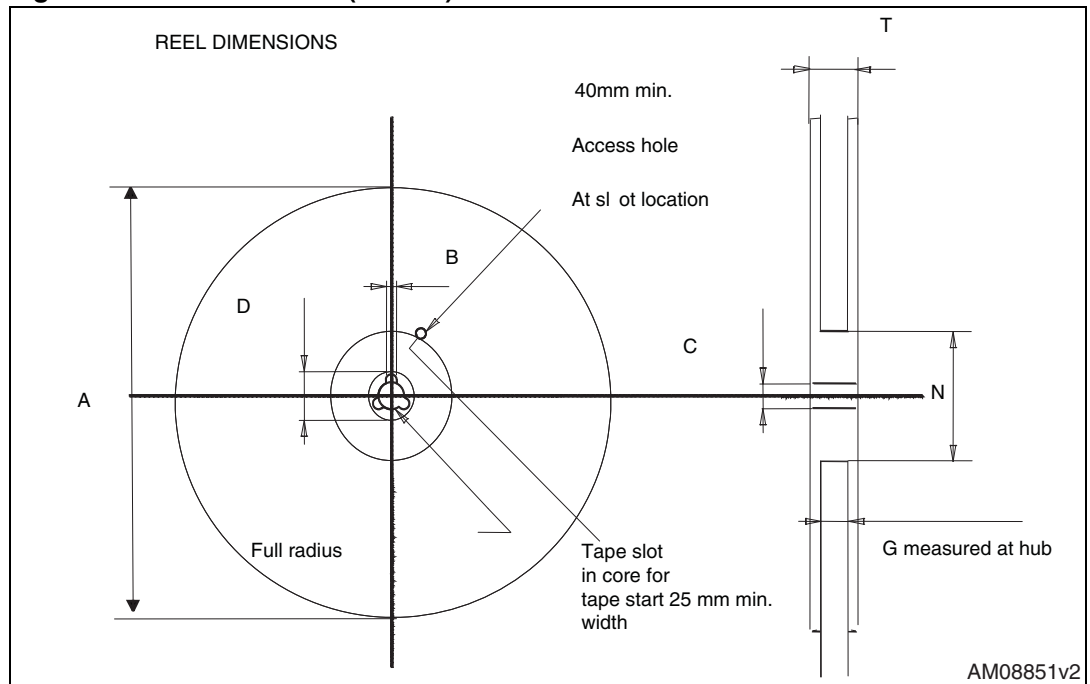


Figure 23. Reel for DPAK (TO-252)



## 6 Revision history

**Table 9. Revision history**

Date	Revision	Changes
11-May-2005	1	First release
31-Jan-2006	2	New template
05-Oct-2011	3	<i>Section : Applications</i> has been modified Minor text changes

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