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TPS54232DR

Texas instruments

Switching Voltage Regulators 2A,28V,1MHz Step Down SWIFT DC/DC

TPS54232 2-A, 28-V, 1-MHz, Step-Down DC-DC Converter With Eco-Mode™

1 Features

- 3.5-V to 28-V Input Voltage Range
- Adjustable Output Voltage Down to 0.8 V
- Integrated 80-mΩ High-Side MOSFET Supports up to 2-A Continuous Output Current
- High Efficiency at Light Loads with a Pulse-Skipping Eco-Mode™
- Fixed 1-MHz Switching Frequency
- Typical 1-μA Shutdown Quiescent Current
- Adjustable Slow-Start Limits Inrush Currents
- Programmable UVLO Threshold
- Overvoltage Transient Protection
- Cycle-by-Cycle Current Limit, Frequency Fold Back and Thermal Shutdown Protection
- Available in 8-Pin SOIC Package
- Supported by WEBENCH® Software Tool (http://www.ti.com/lsds/ti/analog/webench/overview.page)

2 Applications

- Consumer Applications such as Set-Top Boxes, CPE Equipment, LCD Displays, Peripherals, and Battery Chargers
- Industrial and Car Audio Power Supplies
- 5-V, 12-V, and 24-V Distributed Power Systems

3 Description

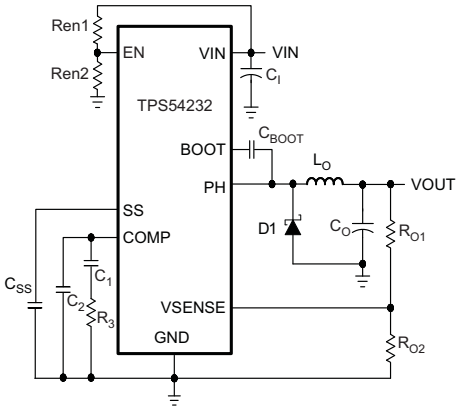
The TPS54232 is a 28-V, nonsynchronous buck converter that integrates a low $R_{DS(on)}$ high-side MOSFET. To increase efficiency at light loads, a pulse-skipping Eco-Mode feature is automatically activated. Furthermore, the 1-μA shutdown supply current allows the device to be used in battery-powered applications. Current mode control with internal slope compensation simplifies the external compensation calculations and reduces component count while allowing the use of ceramic output capacitors. A resistor divider programs the hysteresis of the input undervoltage lockout. An overvoltage transient protection circuit limits voltage overshoots during startup and transient conditions. A cycle-by-cycle current limit scheme, frequency fold back, and thermal shutdown protect the device and the load in the event of an overload condition. The TPS54232 is available in an 8-pin SOIC package.

Device Information(1)

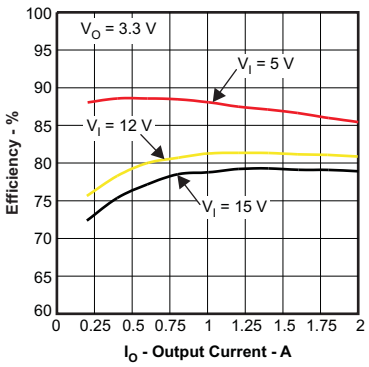
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54232	SOIC (8)	4.90 mm x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Efficiency



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2013) to Revision D — **Page**

- Changed the data sheet to the new standard format ... 1
- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added the *Thermal Information* table ... 6
- Deleted *Package Dissipation Ratings* table ... 7
- Changed Equation 7 ... 15
- Changed Equation 32 ... 20
- Changed Equation 33 ... 20

Changes from Revision B (February 2011) to Revision C — **Page**

- Removed Swift™ from the data sheet title ... 1
- Changed text From: "Where N_C is the number of output capacitors in parallel." To: ":Where C_O is the number of output capacitors in parallel." Following Equation 13 ... 17
- Changed Equation 26 ... 18
- Changed Equation 29 ... 19
- Changed: Switching loss: Paw = 0.5 x 10^{-9} x VIN^2 x I_{OUT} x Few To: Switching loss: Psw = 0.5 x 10^{-9} x VIN^2 x I_{OUT} x Fsw ... 21
- Changed: Gate charge loss: P.C. = 22.8 x 10^{-9} x Few To: Gate charge loss: Pgc. = 22.8 x 10^{-9} x Fsw ... 21
- Deleted graph "Maximum Power Dissipation vs Junction Temperature" from the Supplemental Application Curves ... 22

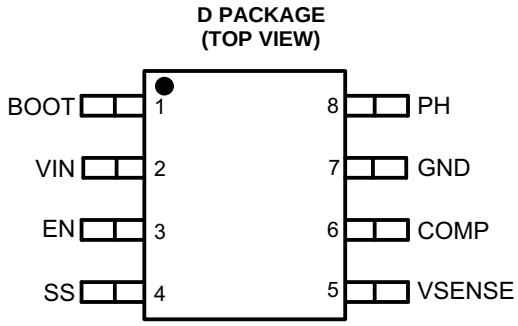
Changes from Revision A (March 2010) to Revision B **Page**

- Deleted feature Item: For SWIFT™ Documentation, See the TI Website at www.ti.com/swift 1
- Changed Figure 14 x-axis From: I_O - Output Current - mA To: I_O - Output Current - A 22

Changes from Original (November 2008) to Revision A **Page**

- Changed Changed the ABSOLUTE MAXIMUM RATINGS table, Input Voltage - EN pin max value From: 5V to 6V 5
- Added a new table to the Description - For additional design needs 14

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A 0.1-µF bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor falls below the minimum requirement, the high-side MOSFET is forced to switch off until the capacitor is refreshed.
VIN	2	I	Input supply voltage, 3.5 V to 28 V.
EN	3	I	Enable pin. Pull below 1.25 V to disable. Float to enable. Programming the input undervoltage lockout with two resistors is recommended.
SS	4	I	Slow start pin. An external capacitor connected to this pin sets the output rise time.
VSENSE	5	I	Inverting node of the gm error amplifier.
COMP	6	O	Error amplifier output, and input to the PWM comparator. Connect frequency compensation components to this pin.
GND	7	-	Ground.
PH	8	O	The source of the internal high-side power MOSFET.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage	VIN	–0.3	30	V
	EN	–0.3	6	
	BOOT		38	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	SS	–0.3	3	
Output Voltage	BOOT-PH	8	8	V
	PH	–0.6	30	
	PH (10 ns transient from ground to negative peak)		–5	
Source Current	EN		100	µA
	BOOT		100	mA
	VSENSE		10	µA
	PH		6	A
Sink Current	VIN		6	A
	COMP		100	µA
	SS		200	
Operating Junction Temperature, T_J		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Operating Input Voltage on (VIN pin)	3.5	28	V
T_J	Operating junction temperature	–40	150	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS54232	UNIT
		D	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	57.1	
ψ_{JT}	Junction-to-top characterization parameter	12.9	
ψ_{JB}	Junction-to-board characterization parameter	56.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 3.5V to 28V (unless otherwise noted)

DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Internal undervoltage lockout threshold	Rising and Falling			3.5	V
Shutdown supply current	EN = 0V, VIN = 12V, –40°C to 85°C		1	4	µA
Operating – non switching supply current	VSENSE = 0.85 V		85	120	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising and Falling		1.25	1.35	V
Input current	Enable threshold – 50 mV		-1		µA
Input current	Enable threshold + 50 mV		-4		µA
VOLTAGE REFERENCE					
Voltage reference		0.772	0.8	0.828	V
HIGH-SIDE MOSFET					
On resistance	BOOT-PH = 3 V, VIN = 3.5 V		115	200	mΩ
	BOOT-PH = 6 V, VIN = 12 V		80	150	
ERROR AMPLIFIER					
Error amplifier transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		92		µmhos
Error amplifier DC gain(1)	VSENSE = 0.8 V		800		V/V
Error amplifier unity gain bandwidth(1)	5 pF capacitance from COMP to GND pins		2.7		MHz
Error amplifier source/sink current	$V_{(COMP)}$ = 1.0 V, 100 mV overdrive		±7		µA
Switch current to COMP transconductance	VIN = 12 V		10		A/V
PULSE-SKIPPING ECO-MODE					
Pulse-skipping Eco-Mode switch current threshold			100		mA
CURRENT LIMIT					
Current limit threshold	VIN = 12 V	2.3	4.9		A
THERMAL SHUTDOWN					
Thermal Shutdown			165		°C
SLOW START (SS PIN)					
Charge current	$V_{(SS)}$ = 0.4 V		2		µA
SS to VSENSE matching	$V_{(SS)}$ = 0.4 V		10		mV

(1) Specified by design

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS54232 Switching Frequency	VIN = 12V, 25°C	800	1000	1200	kHz
Minimum controllable on time	VIN = 12V, 25°C		110	135	ns
Maximum controllable duty ratio(1)	BOOT-PH = 6 V	90%	93%		

(1) Specified by design

7.7 Typical Characteristics

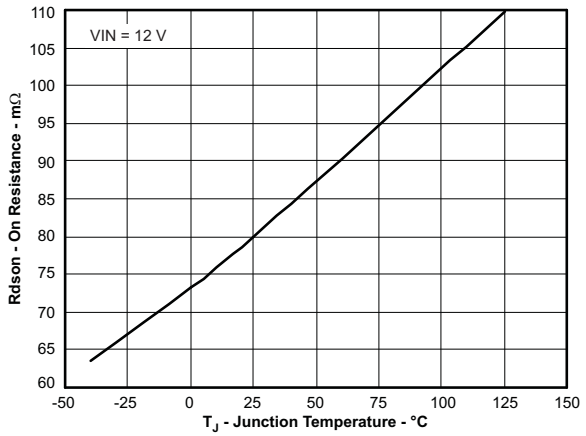


Figure 1. On Resistance vs Junction Temperature

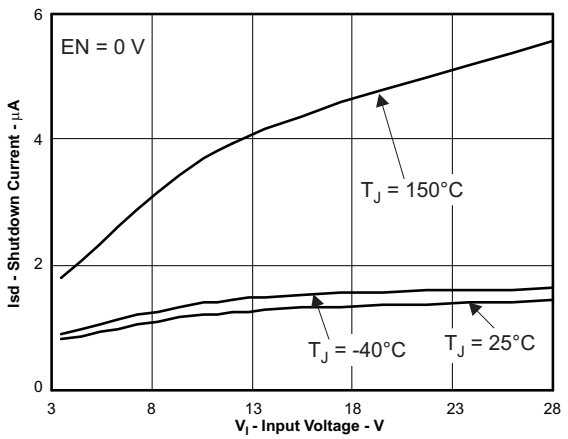


Figure 2. Shutdown Quiescent Current vs Input Voltage

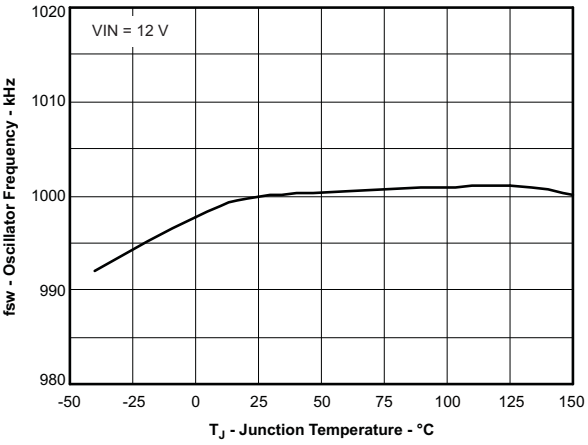


Figure 3. Switching Frequency vs Junction Temperature

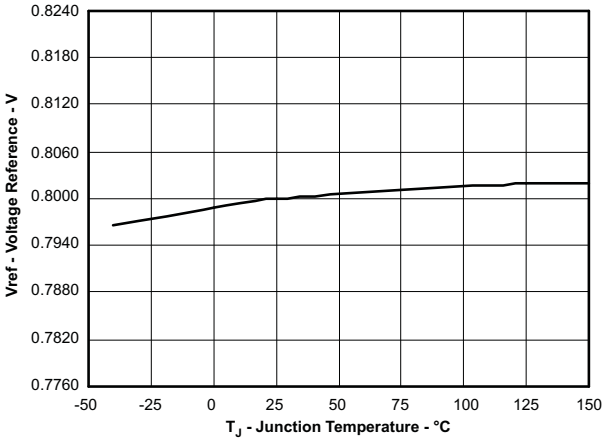


Figure 4. Voltage Reference vs Junction Temperature

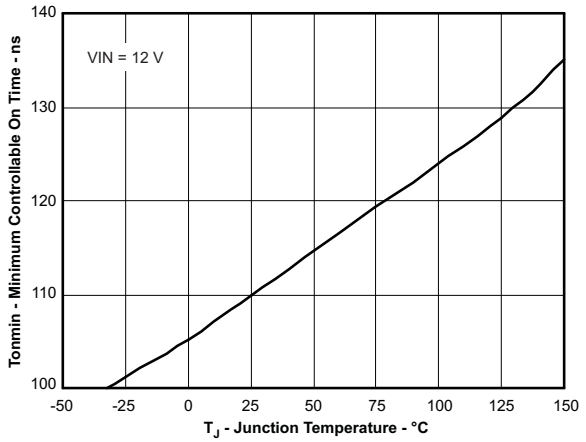


Figure 5. Minimum Controllable On Time vs Junction Temperature

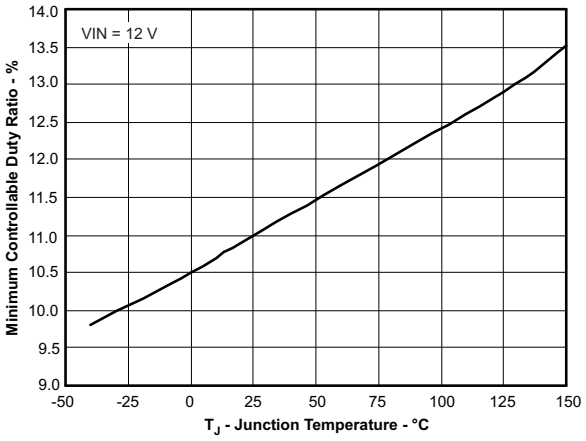


Figure 6. Minimum Controllable Duty Ratios Junction Temperature

Typical Characteristics (continued)

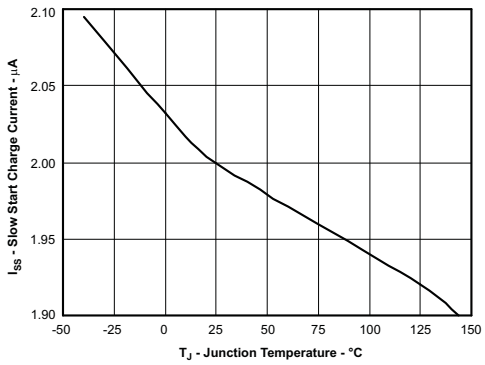


Figure 7. SS Charge Current vs Junction Temperature

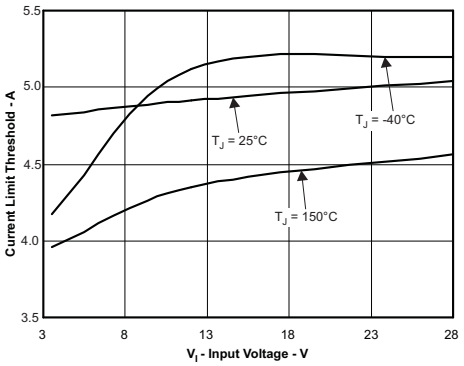


Figure 8. Current Limit Threshold vs Input Voltage

8 Detailed Description

8.1 Overview

The TPS54232 is a 28-V, 2-A, step-down (buck) converter with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design. The TPS54232 has a pre-set switching frequency of 1MHz.

The TPS54232 needs a minimum input voltage of 3.5 V to operate normally. The EN pin has an internal pull-up current source that can be used to adjust the input-voltage, undervoltage lockout (UVLO) with two external resistors. In addition, the pull-up current provides a default condition when the EN pin is floating for the device to operate. The operating current is 85 µA typically when not switching and under no load. When the device is disabled, the supply current is 1 µA typically.

The integrated 80-mΩ high-side MOSFET allows for high efficiency power supply designs with continuous output currents up to 2 A.

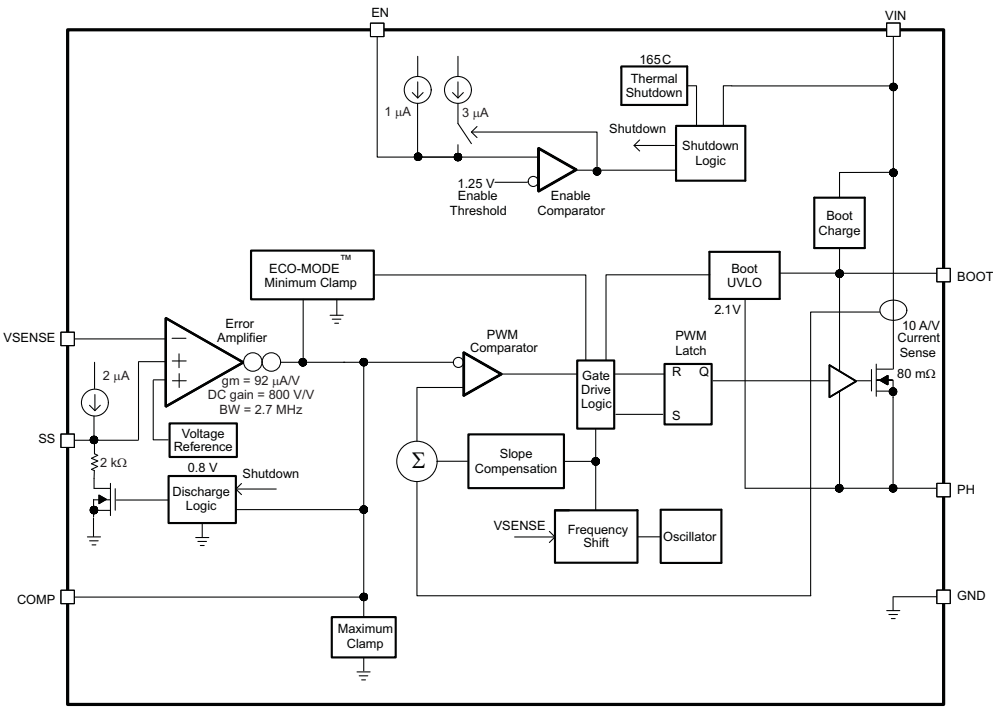
The TPS54232 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V typically. The output voltage can be stepped down to as low as the reference voltage.

By adding an external capacitor, the slow start time of the TPS54232 can be adjustable which enables flexible output filter selection.

To improve the efficiency at light load conditions, the TPS54232 enters a special pulse-skipping Eco-Mode when the peak inductor current drops below 100 mA typically.

The frequency foldback reduces the switching frequency during startup and over current conditions to help control the inductor current. The thermal shut down gives the additional protection under fault conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed-Frequency PWM Control

The TPS54232 uses a fixed frequency, peak current mode control. The internal switching frequency of the TPS54232 is fixed at 1 MHz.

8.3.2 Voltage Reference (V_{ref})

The voltage reference system produces a ±2% initial accuracy voltage reference (±3.5% over temperature) by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.8 V.

8.3.3 Bootstrap Voltage (BOOT)

The TPS54232 has an integrated boot regulator and requires a 0.1-µF ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS54232 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.1 V typically.

8.3.4 Enable and Adjustable Input Undervoltage Lockout (VIN UVLO)

The EN pin has an internal pull-up current source that provides the default condition of the TPS54232 operating when the EN pin floats.

The TPS54232 is disabled when the VIN pin voltage falls below internal VIN UVLO threshold. It is recommended to use an external VIN UVLO to add hysteresis unless VIN is greater than (V_{OUT} + 2V). To adjust the VIN UVLO with hysteresis, use the external circuitry connected to the EN pin as shown in Figure 9. Once the EN pin voltage exceeds 1.25 V, an additional 3 µA of hysteresis is added. Use Equation 1 and Equation 2 to calculate the resistor values needed for the desired VIN UVLO threshold voltages. The V_{START} is the input start threshold voltage, the V_{STOP} is the input stop threshold voltage and the V_{EN} is the enable threshold voltage of 1.25 V. The V_{STOP} should always be greater than 3.5 V.

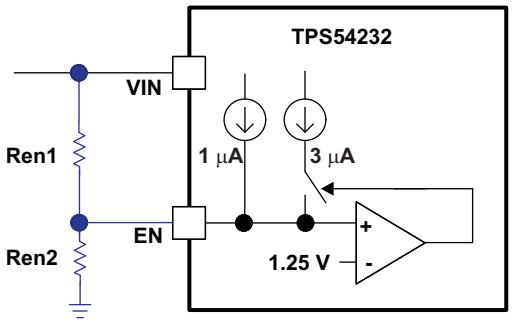


Figure 9. Adjustable Input Undervoltage Lockout

$$Ren1 = \frac{V_{START} - V_{STOP}}{3\ \mu A} \quad (1)$$

$$Ren2 = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{Ren1} + 1\ \mu A} \quad (2)$$

8.3.5 Programmable Slow-Start Using SS Pin

It is highly recommended to program the slow start time externally because no slow start time is implemented internally. The TPS54232 effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the power supply's reference voltage fed into the error amplifier and will regulate the output accordingly. A capacitor (C_{SS}) on the SS pin to ground implements a slow start time. The TPS54232 has an internal pull-up current source of 2 µA that charges the external slow start capacitor. The equation for the slow start time (10% to 90%) is shown in Equation 3. The V_{ref} is 0.8V and the I_{SS} current is 2µA.

Feature Description (continued)

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times V_{ref}(V)}{I_{SS}(\mu A)} \quad (3)$$

The slow start time should be set between 1 ms to 10 ms to ensure good startup behavior. The slow-start capacitor should be no more than 27 nF.

If during normal operation, the input voltage drops below the VIN UVLO threshold, or the EN pin is pulled below 1.25 V, or a thermal shutdown event occurs, the TPS54232 stops switching.

8.3.6 Error Amplifier

The TPS54232 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 92 µA/V during normal operation. Frequency compensation components are connected between the COMP pin and ground.

8.3.7 Slope Compensation

In order to prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the TPS54232 adds a built-in slope compensation which is a compensating ramp to the switch current signal.

8.3.8 Current Mode Compensation Design

For designs using ceramic output capacitors, proper derating of ceramic output capacitance is recommended when doing the stability analysis. This is because the actual ceramic capacitance drops considerably from the nominal value when the applied voltage increases. For the detailed guidelines, see the *Detailed Design Procedure* section.

8.3.9 Overcurrent Protection and Frequency Shift

The TPS54232 implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle by cycle basis. Every cycle the switch current and the COMP pin voltage are compared; when the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limit the output current.

The TPS54232 provides robust protection during short circuits. There is potential for overcurrent runaway in the output inductor during a short circuit at the output. The TPS54232 solves this issue by increasing the off time during short circuit conditions by lowering the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 V to 0.8 V on VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is shown in Table 1.

Table 1. Switching Frequency Conditions

SWITCHING FREQUENCY	VSENSE PIN VOLTAGE
1 MHz	VSENSE ≥ 0.6 V
1 MHz / 2	0.6 V > VSENSE ≥ 0.4 V
1 MHz / 4	0.4 V > VSENSE ≥ 0.2 V
1 MHz / 8	0.2 V > VSENSE

8.3.10 Overvoltage Transient Protection

The TPS54232 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above 109% × V_{ref}, the high-side MOSFET will be forced off. When the VSENSE pin voltage falls below 107% × V_{ref}, the high-side MOSFET will be enabled again.

8.3.11 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 165°C, the device reinitiates the power up sequence.

8.4 Device Functional Modes

8.4.1 Eco-Mode

The TPS54232 device is designed to operate in pulse skipping Eco-mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 100 mA (typical), the COMP pin voltage falls to 0.5 V (typical) and the device enters Eco-mode . When the device is in Eco-mode, the COMP pin voltage is clamped at 0.5 V internally which prevents the high-side integrated MOSFET from switching. The peak inductor current must rise above 100 mA for the COMP pin voltage to rise above 0.5 V and exit Eco-mode. Because the integrated current comparator catches the peak inductor current only, the average load current entering Eco-mode varies with the applications and external output filters.

8.4.2 Operation With VIN < 3.5 V

The device is recommended to operate with input voltages above 3.5 V. The typical VIN UVLO threshold is not specified and the device can operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device does not switch. If the EN pin is externally pulled up or left floating, the device becomes active when the VIN pin passes the UVLO threshold. Switching begins when the slow-start sequence is initiated.

8.4.3 Operation With EN Control

The enable threshold voltage is 1.25 V (typical). With the EN pin is held below that voltage the device is disabled and switching is inhibited even if the VIN pin is above the UVLO threshold. The IC quiescent current is reduced in this state. If the EN voltage increases above the threshold while the VIN pin is above the UVLO threshold, the device becomes active. Switching is enabled, and the slow-start sequence is initiated.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS54232 device is typically used as a step-down converter, which converts a voltage from 3.5 V to 28 V to a lower voltage. WEBENCH™ software is available to aid in the design and analysis of circuits.

For additional design needs, see:

	TPS54231	TPS54232	TPS54233	TPS54331	TPS54332
I_O(Max)	2A	2A	2A	3A	3.5A
Input Voltage Range	3.5V - 28V	3.5V - 28V	3.5V - 28V	3.5V - 28V	3.5V - 28V
Switching Freq. (Typ)	570kHz	1000kHz	285kHz	570kHz	1000kHz
Swiitch Current Limit (Min)	2.3A	2.3A	2.3A	3.5A	4.2A
Pin/Package	8SOIC	8SOIC	8SOIC	8SOIC	8SO PowerPAD™

9.2 Typical Application

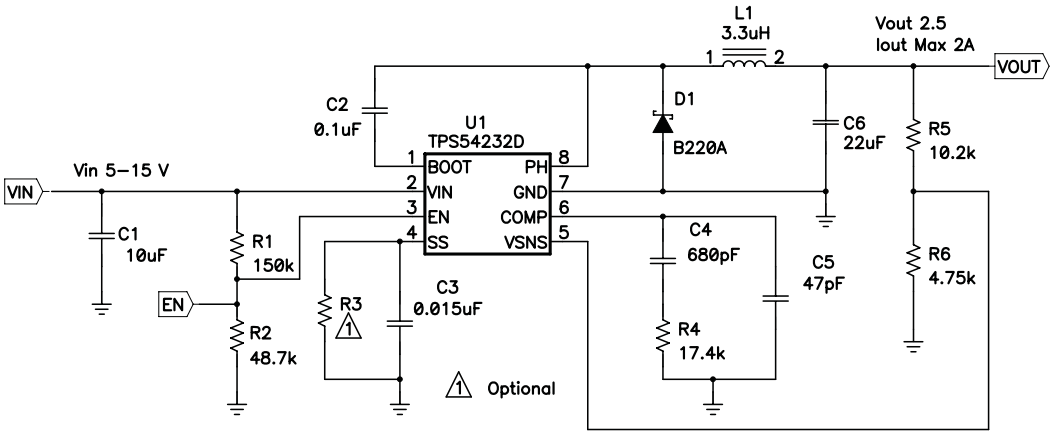


Figure 10. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in Table 2 as the input parameters

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5 V to 15V
Output voltage	2.5 V
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Output current rating	2 A
Operating Frequency	1 MHz

9.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS54232. Alternately, the WEBENCH Software may be used to generate a complete design. The WEBENCH™ Software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

9.2.2.1 Switching Frequency

The switching frequency for the TPS54232 is fixed at 1 MHz.

9.2.2.2 Output Voltage Set Point

The output voltage of the TPS54232 is externally adjustable using a resistor divider network. In the application circuit of Figure 10, this divider network is comprised of R5 and R6. The relationship of the output voltage to the resistor divider is given by Equation 4 and Equation 5.

$$R6 = \frac{R5 \times V_{REF}}{V_{OUT} - V_{REF}} \tag{4}$$

$$V_{OUT} = V_{REF} \times \left[\frac{R5}{R6} + 1\right] \tag{5}$$

Choose R5 to be approximately 10 kΩ. Slightly increasing or decreasing R5 can result in closer output voltage matching when using standard value resistors. In this design, R4 = 10.2 kΩ and R = 4.75 kΩ, resulting in a 2.5 V output voltage. The zero ohm resistor R4 is provided as a convenient place to break the control loop for stability testing.

9.2.2.3 Input Capacitors

The TPS54232 requires an input decoupling capacitor and depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value may be used as long as all other requirements are met; however 10 µF has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be needed, especially if the TPS54232 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design a 10 µF capacitor issued for the input decoupling capacitor. It isX5R dielectric rated for 25 V. The equivalent series resistance (ESR) is approximately 5 mΩ, and the current rating is 3 A.

This input ripple voltage can be approximated by Equation 6.

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \tag{6}$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency, C_{BULK} is the input capacitor value and ESR_{MAX} is the maximum series resistance of the input capacitor.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by Equation 7.

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \tag{7}$$

In this case, the input ripple voltage would be 60 mV and the RMS ripple current would be 1 A. It is also important to note that the actual input voltage ripple will be greatly affected by parasitics associated with the layout and the output impedance of the voltage source. The actual input voltage ripple for this circuit is shown in Table 2 and is larger than the calculated value. This measured value is still below the specified input limit of 300 mV. The maximum voltage across the input capacitors would be VIN max plus ΔVIN/2. The chosen bulk and bypass capacitors are each rated for 25 V and the ripple current capacity is greater than 3 A, both providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

9.2.2.4 Output Filter Components

Two components need to be selected for the output filter, L1 and C3. Since the TPS54232 is an externally compensated device, a wide range of filter component types and values can be supported.

9.2.2.4.1 Inductor Selection

To calculate the minimum value of the output inductor, use Equation 8.

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW}} \quad (8)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, this value is at the discretion of the designer; however, the following guidelines may be used. For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.4 may be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.35 and the minimum inductor value is calculated to be 2.97 µH. For this design, a large value was chosen: 3.3 µH.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The peak-to-peak inductor current is calculated using Equation 9.

$$I_{LPP} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times 0.8} \quad (9)$$

The RMS inductor current can be found from Equation 10.

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}\right)^2} \quad (10)$$

and the peak inductor current can be determined with Equation 11.

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (11)$$

For this design, the RMS inductor current is 2.01 A and the peak inductor current is 2.39 A. The chosen inductor is a Coilcraft MSS7341-332NL 3.3 µH. It has a saturation current rating of 3.28 A and an RMS current rating of 3.95 A, meeting these requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wishes to allow so long as the other design requirements are met. Larger value inductors will have lower ac current and result in lower output voltage ripple, while smaller inductor values will increase ac current and output voltage ripple. Inductor values for use with the TPS54232 are in the range of 1 µH to 47 µH.

9.2.2.4.2 Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the closed loop crossover frequency at less than 1/5 of the switching frequency. With high-switching frequencies such as the 1 MHz frequency of this design, internal circuit limitations of the TPS54232 limit the practical maximum crossover frequency to about 70 kHz. In general, the closed loop crossover frequency should be higher than the corner frequency determined by the load impedance and the output capacitor. This limits the minimum capacitor value for the output filter to:

$$C_{O\_min} = 1/(2 \times \pi \times R_O \times F_{CO\_max}) \quad (12)$$

Where R_O is the output load impedance (V_O/I_O) and f_{CO} is the desired crossover frequency. For a desired maximum crossover of 50 kHz the minimum value for the output capacitor is around 2.5 µF. This may not satisfy the output ripple voltage requirement. The output ripple voltage consists of two components; the voltage change due to the charge and discharge of the output filter capacitance and the voltage change due to the ripple current times the ESR of the output filter capacitor. The output ripple voltage can be estimated by:

$$V_{OPP} = I_{LPP}\left[\frac{(D-0.5)}{4 \times F_{SW} \times C_O} + R_{ESR}\right] \quad (13)$$

The maximum ESR of the output capacitor can be determined from the amount of allowable output ripple as specified in the initial design parameters. The contribution to the output ripple voltage due to ESR is the inductor ripple current times the ESR of the output filter, so the maximum specified ESR as listed in the capacitor data sheet is given by Equation 14.

$$ESR_{max} = \frac{V_{OPPMAX}}{I_{LPP}} - \frac{(D-0.5)}{4 \times F_{SW} \times C_O} \quad (14)$$

Where V_{OPPMAX} is the desired maximum peak-to-peak output ripple. The maximum RMS ripple current in the output capacitor is given by Equation 15.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C}\right) \quad (15)$$

Where N_C is the number of output capacitors in parallel.

For this design example, a single 22-µF ceramic output capacitor is chosen for C6. It is rated at 10 V with a maximum ESR of 5 mΩ and a ripple current rating in excess of 3 A. The calculated total RMS ripple current is 182 mA and the maximum total ESR required is 51 mΩ. This output capacitor exceeds the requirements by a wide margin and will result in a reliable, high-performance design. it is important to note that the actual capacitance in circuit may be less than the catalog value when the output is operating near the rated voltage for the capacitor. The selected output capacitor must be rated for a voltage greater than the desired output voltage plus ½ the ripple voltage but in this example a 10-V capacitor is used so that the effective capacitance will remain close to the stated value of 22 µF. Other capacitor types work well with the TPS54232, depending on the needs of the application.

9.2.2.5 Compensation Components

The external compensation used with the TPS54232 allows for a wide range of output filter configurations. A large range of capacitor values and types of dielectric are supported. The design example uses a ceramic X5R dielectric output capacitor, but other types are supported.

A Type II compensation scheme is recommended for the TPS54232. The compensation components are chosen to set the desired closed loop cross over frequency and phase margin for output filter components. The type II compensation has the following characteristics; a dc gain component, a low frequency pole, and a mid frequency zero / pole pair.

The DC gain is determined by Equation 16.

$$G_{DC} = \frac{V_{ggm} \times V_{REF}}{V_O} \quad (16)$$

Where:

V_{ggm} = 800
V_{REF} = 0.8 V

The low-frequency pole is determined by Equation 17.

$$V_{PO} = 1/(2 \times \pi \times R_{OO} \times C_Z) \quad (17)$$

The mid-frequency zero is determined by Equation 18.

$$F_{Z1} = 1/\left(2 \times \pi \times R_Z \times C_Z\right) \quad (18)$$

And, the mid-frequency pole is given by Equation 19.

$$F_{P1} = 1/\left(2 \times \pi \times R_Z \times C_P\right) \quad (19)$$

The first step is to choose the closed loop crossover frequency. In general, the closed-loop crossover frequency should be less than 1/8 of the minimum operating frequency, but for the TPS54232 it is recommended that the maximum closed loop crossover frequency be not greater than 75 kHz. Next, the required gain and phase boost of the crossover network needs to be calculated. By definition, the gain of the compensation network must be the inverse of the gain of the modulator and output filter. For this design example, where the ESR zero is much higher than the closed loop crossover frequency, the gain of the modulator and output filter can be approximated by Equation 20.

$$\text{Gain} = -20\log\left(2 \times \pi \times R_{SENSE} \times F_{CO} \times C_O\right) - 2\text{dB} \quad (20)$$

Where:

R_{SENSE} = 1Ω/10
F_{CO} = Closed-loop crossover frequency
C_O = Output capacitance

The phase loss is given by Equation 21.

$$PL = a\tan\left(2 \times \pi \times F_{CO} \times R_{ESR} \times C_O\right) - a\tan\left(2 \times \pi \times F_{CO} \times R_O \times C_O\right) - 10\text{deg} \quad (21)$$

Where:

R_{ESR} = Equivalent series resistance of the output capacitor
$R_O = V_O/I_O$

The measured overall loop response for the circuit is given in Figure 20. Note that the actual closed-loop crossover frequency is higher than intended at about 25 kHz. This is primarily due to variation in the actual values of the output filter components and tolerance variation of the internal feed-forward gain circuitry. Overall the design has greater than 60 degrees of phase margin and will be completely stable over all combinations of line and load variability.

Now that the phase loss is known the required amount of phase boost to meet the phase margin requirement can be determined. The required phase boost is given by Equation 22.

$$PB = \left(PM - 90\,\text{deg}\right) - PL \quad (22)$$

Where PM = the desired phase margin.

A zero / pole pair of the compensation network will be placed symmetrically around the intended closed loop frequency to provide maximum phase boost at the crossover point. The amount of separation can be determined by Equation 23 and the resultant zero and pole frequencies are given by Equation 24 and Equation 25.

$$k = \tan\left(\frac{PB}{2} + 45\,\text{deg}\right) \quad (23)$$

$$F_{Z1} = \frac{F_{CO}}{k} \quad (24)$$

$$F_{P1} = F_{CO} \times k \quad (25)$$

The low-frequency pole is set so that the gain at the crossover frequency is equal to the inverse of the gain of the modulator and output filter. Due to the relationships established by the pole and zero relationships, the value of R_Z can be derived directly by Equation 26.

$$R_Z = \frac{2 \times \pi \times F_{CO} \times V_O \times C_O \times R_{OA} \times 0.754}{GM_{ICOMP} \times V_{ggm} \times V_{REF}} \quad (26)$$

Where:

V_O = Output voltage
C_O = Output capacitance
F_{CO} = Desired crossover frequency
R_{OA} = 8.696 MΩ
GM_{COMP} = 10 A/V
V_{ggm} = 800
V_{REF} = 0.8 V

With R_Z known, C_Z and C_P can be calculated using Equation 27 and Equation 28.

$$C_Z = \frac{1}{2 \times \pi \times F_{Z1} \times R_z} \quad (27)$$

$$C_P = \frac{1}{2 \times \pi \times F_{P1} \times R_z} \quad (28)$$

For this design, a 22-µF output capacitor issued. For ceramic capacitors, the actual output capacitance is less than the rated value when the capacitors have a dc bias voltage applied. This is the case in a DC - DC converter. For this design, a 10-V capacitor is chosen to minimize this effect. The ESR is approximately 0.005 Ω.

Using Equation 20 and Equation 21, the output stage gain and phase loss are equivalent as:

Gain = 1.613 dB
and
PL = -92.3 degrees

For 60 degrees of phase margin, Equation 22 requires 62.33 degrees of phase boost.

Equation 23, Equation 24, and Equation 25 are used to find the zero and pole frequencies of:

F_{Z1} = 12.3 k Hz

And

F_{P1} = 203 kHz

R_Z, C_Z, and C_P are calculated using Equation 26, Equation 27, and Equation 28.

$$Rz = \frac{2 \times \pi \times 50000 \times 2.5 \times 22 \times 10^{-6} \times 8.696 \times 10^{6} \times 0.754}{10 \times 800 \times 0.8} = 17.7\ k\Omega \quad (29)$$

$$Cz = \frac{1}{2 \times \pi \times 12300 \times 17700} = 730\ pF \quad (30)$$

$$Cp = \frac{1}{2 \times \pi \times 203000 \times 17700} = 44\ pF \quad (31)$$

Using standard values for R3, C6, and C7 in the application schematic of Figure 10:

R3 = 17.4 kΩ
C6 = 680 pF
C7 = 47 pF

9.2.2.6 Bootstrap Capacitor

Every TPS54232 design requires a bootstrap capacitor, C4. The bootstrap capacitor must be 0.1 µF. The bootstrap capacitor is located between the PH pins and BOOT pin. The bootstrap capacitor should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

9.2.2.7 Catch Diode

The TPS54232 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is $VIN_{(MAX)}$ + 0.5 V. Peak current must be greater than IOUTMAX plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B220A is chosen, with a reverse voltage of 20 V, forward current of 2 A, and a forward voltage drop of 0.5 V.

9.2.2.8 Output Voltage Limitations

Due to the internal design of the TPS54232, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 90% and is given by Equation 32.

$$V_{O(max)} = 0.90 \times ((V_{IN(min)} - I_{O(max)} \times R_{dson(max)}) + V_D) - (I_{O(max)} \times R_L) - V_D \quad (32)$$

Where:

$V_{IN(min)}$ = Minimum input voltage
$I_{O(max)}$ = Maximum load current
V_D = Catch diode forward voltage
R_L = Output inductor series resistance

The equation assumes maximum on resistance for the internal high-side FET.

The lower limit is constrained by the minimum controllable on time which may be as high as 135 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by Equation 33.

$$V_{O(min)} = 0.162 \times ((V_{IN(max)} - I_{O(min)} \times R_{dson(min)}) + V_D) - (I_{O(min)} \times R_L) - V_D \quad (33)$$

Where:

$V_{IN(max)}$ = Maximum input voltage
$I_{O(min)}$ = Minimum load current
V_D = Catch diode forward voltage
R_L = Output inductor series resistance

This equation assumes nominal on-resistance for the high-side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to assure proper functionality.

9.2.2.9 Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working in the discontinuous conduction mode (DCM) or pulse-skipping Eco-Mode.

The device power dissipation includes:

1. Conduction loss: Pcon = I_{OUT}^2 x $R_{DS(on)}$ x V_{OUT}/VIN
2. Switching loss: Psw = 0.5 x 10^{-9} x VIN^2 x I_{OUT} x Fsw
3. Gate charge loss: Pgc. = 22.8 x 10^{-9} x Fsw
4. Quiescent current loss: Pq = 0.085 x 10^{-3} x VIN

Where:

I_{OUT} is the output current (A).
$R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).
V_{OUT} is the output voltage (V).
VIN is the input voltage (V).
Fsw is the switching frequency (Hz).

So:

Ptot = Pcon + Psw + Pgc + Pq
For given T_A , T_J = T_A + Rth x Ptot.
For given T_{JMAX} = 150°C, T_{AMAX} = T_{JMAX}– Rth x Ptot.

Where:

Ptot is the total device power dissipation (W).
T_A is the ambient temperature (°C).
T_J is the junction temperature (°C) .
Rth is the thermal resistance of the package (°C/W).
T_{JMAX} is maximum junction temperature (°C).
T_{AMAX} is maximum ambient temperature (°C).

9.2.3 Application Curves

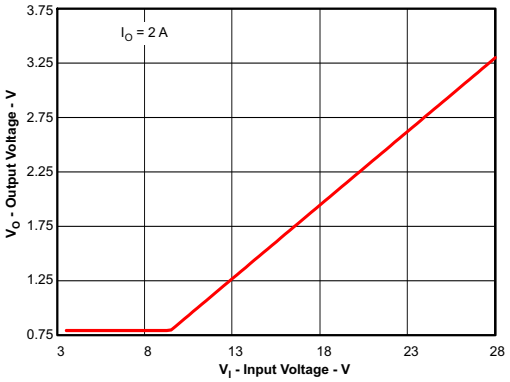


Figure 11. Typical Minimum Output Voltage vs Input Voltage

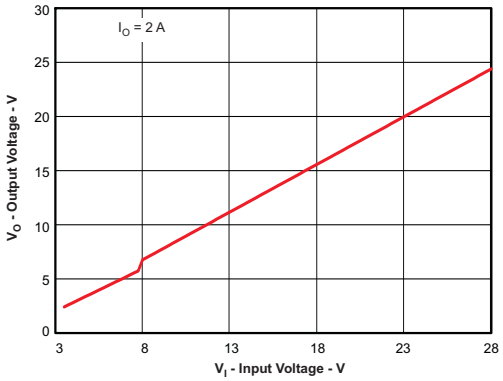


Figure 12. Typical Maximum Output Voltage vs Input Voltage

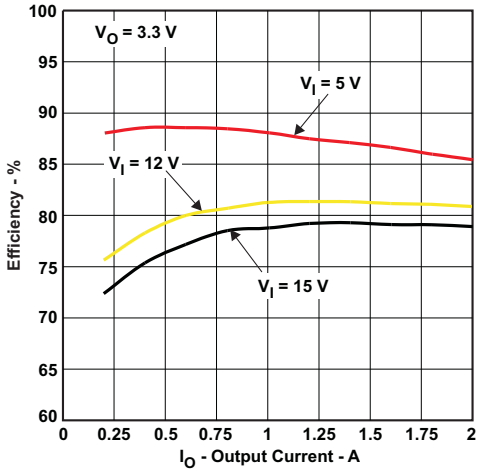


Figure 13. TPS54232 Efficiency

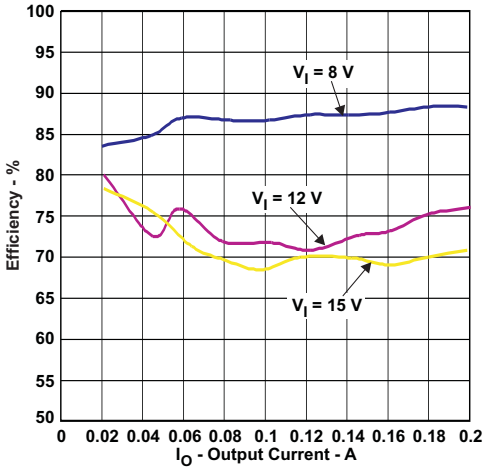


Figure 14. TPS54232 Low Current Efficiency

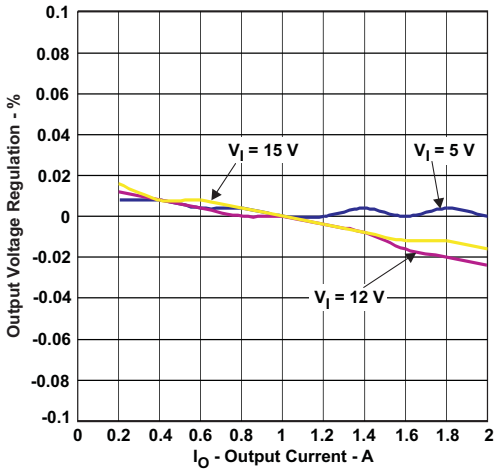


Figure 15. TPS54232 Load Regulation

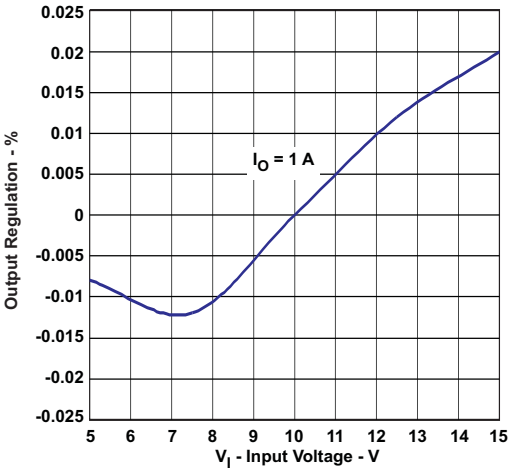


Figure 16. TPS54232 Line Regulation

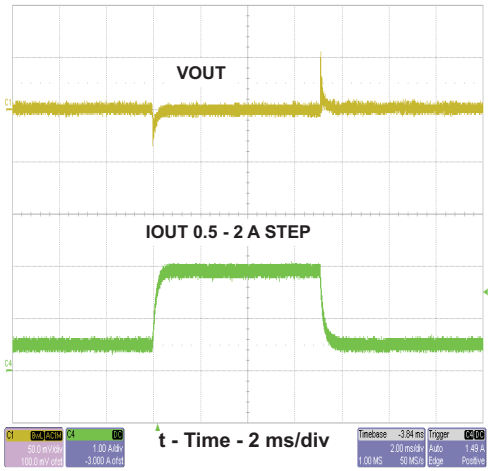


Figure 17. TPS54232 Transient Response

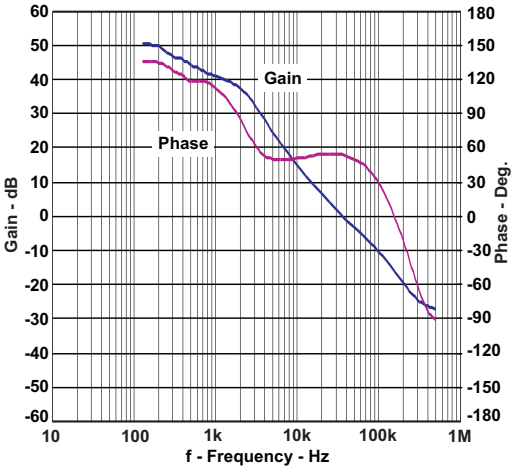


Figure 18. TPS54232 Loop Response

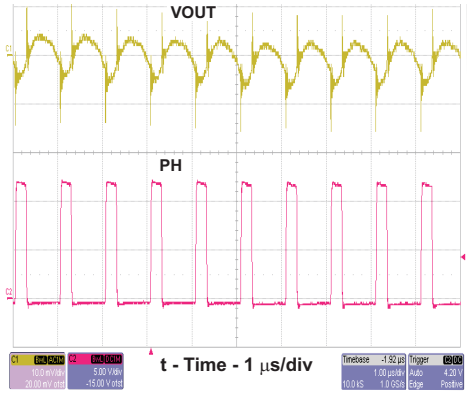


Figure 19. TPS54232 Output Ripple

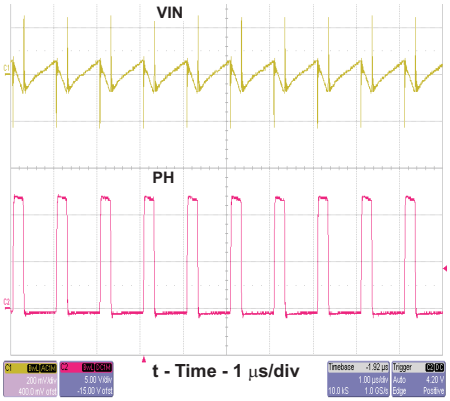


Figure 20. TPS54232 Input Ripple

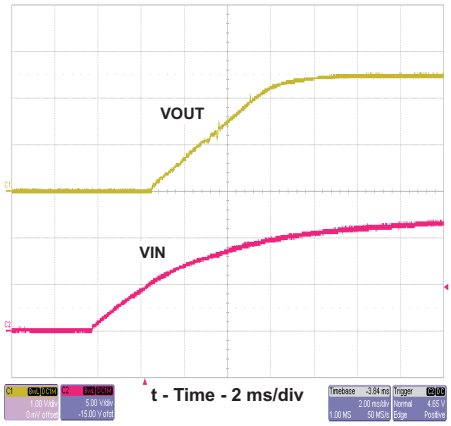


Figure 21. TPS54232 Startup

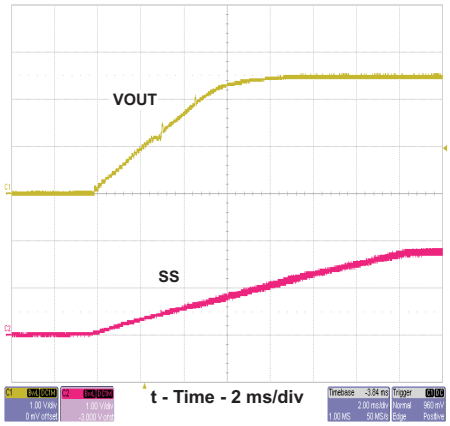


Figure 22. TPS54232 Startup Relative to Enable

10 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 3.5 V and 28 V. This input supply should be well regulated. If the input supply is located more than a few inches from the converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µ F is a typical choice.

11 Layout

11.1 Layout Guidelines

The VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The typical recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the source of the anode of the catch diode. The GND D pin should be tied to the PCB ground plane at the pin of the IC. The source of the low-side MOSFET should be connected directly to the top side PCB ground area used to tie together the ground sides of the input and output capacitors as well as the anode of the catch diode. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Since the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The TPS54232 uses a fused lead frame so that the GND pin acts as a conductive path for heat dissipation from the die. Many applications have larger areas of internal or back side ground plane available, and the top side ground area can be connected to these areas using multiple vias under or adjacent to the device to help dissipate heat. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate layout schemes, however this layout has been shown to produce good results and is intended as a guideline.

11.2 Layout Example

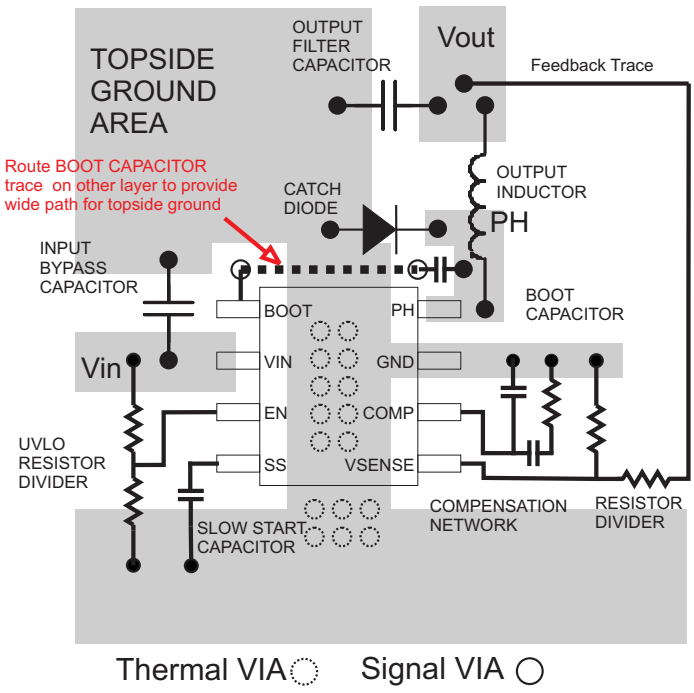


Figure 23. TPS54232 Board Layout

11.3 Estimated Circuit Area

The estimated printed circuit board area for the components used in the design of Figure 10 is 0.44 in^2. This area does not include test points or connectors.

11.4 Electromagnetic Interference (EMI) Considerations

As EMI becomes a rising concern in more and more applications, the internal design of the TPS54232 takes measures to reduce the EMI. The high-side MOSFET gate drive is designed to reduce the PH pin voltage ringing. The internal IC rails are isolated to decrease the noise sensitivity. A package bond wire scheme is used to lower the parasitics effects.

To achieve the best EMI performance, external component selection and board layout are equally important. Follow the *Detailed Design Procedure* above to prevent potential EMI issues.

12 Device And Documentation Support

12.1 Trademarks

Eco-Mode, WEBENCH, PowerPAD are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, And Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	O
TPS54232D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	
TPS54232DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including t
do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in sp
reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm
flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a lin
of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/B
lines if the finish value exceeds the maximum column width.

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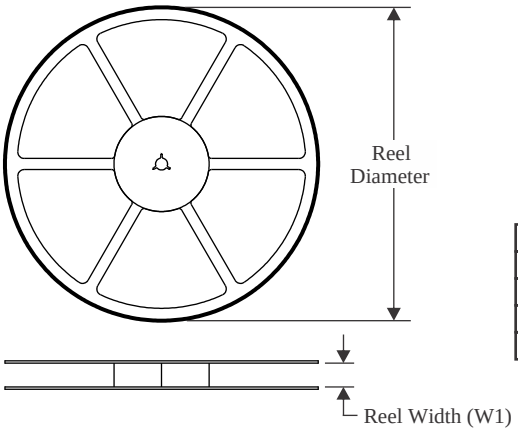
provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis o
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

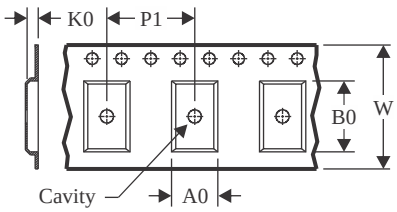
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer o

TAPE AND REEL INFORMATION

REEL DIMENSIONS

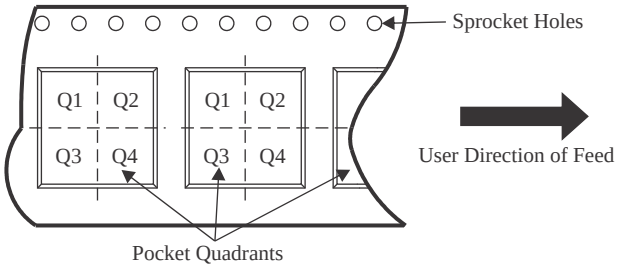


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

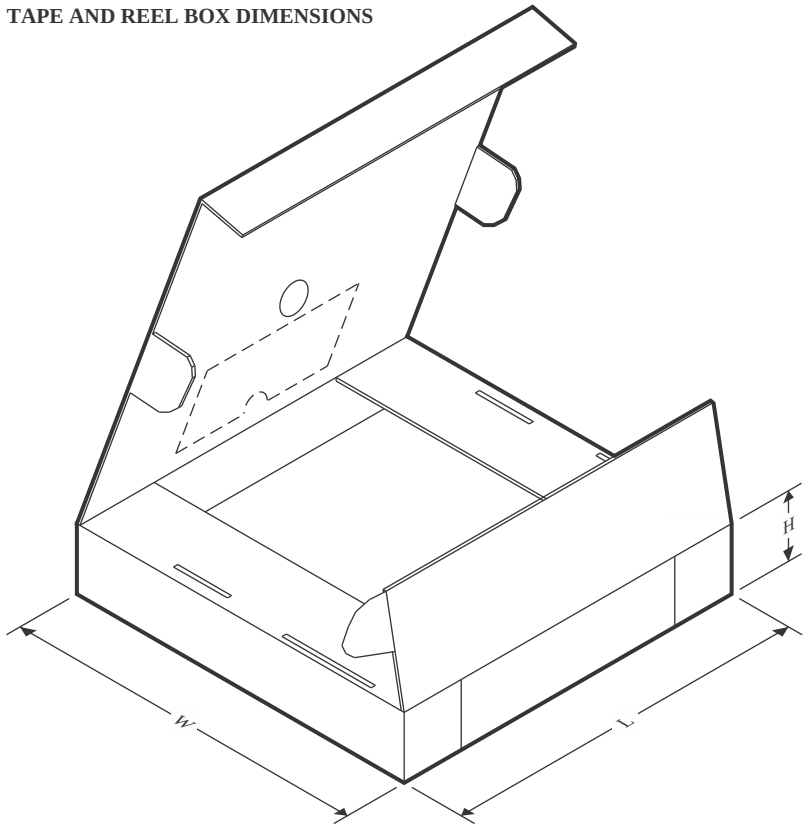
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54232DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

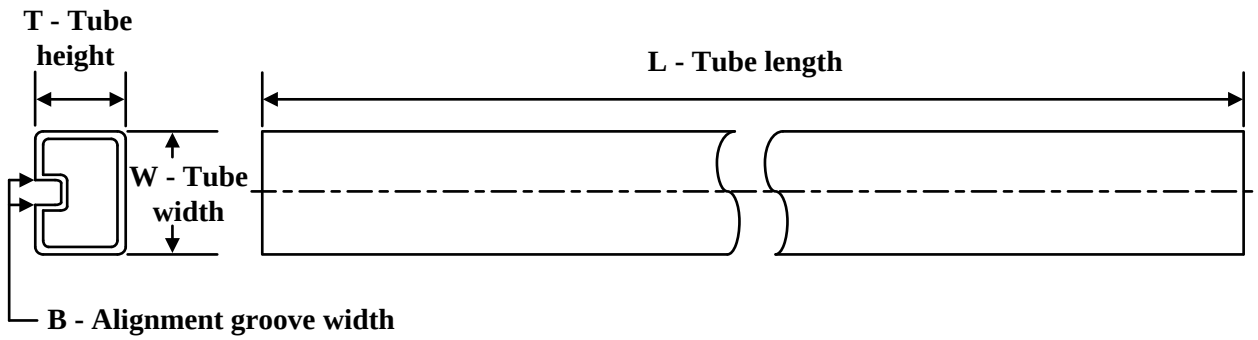
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54232DR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

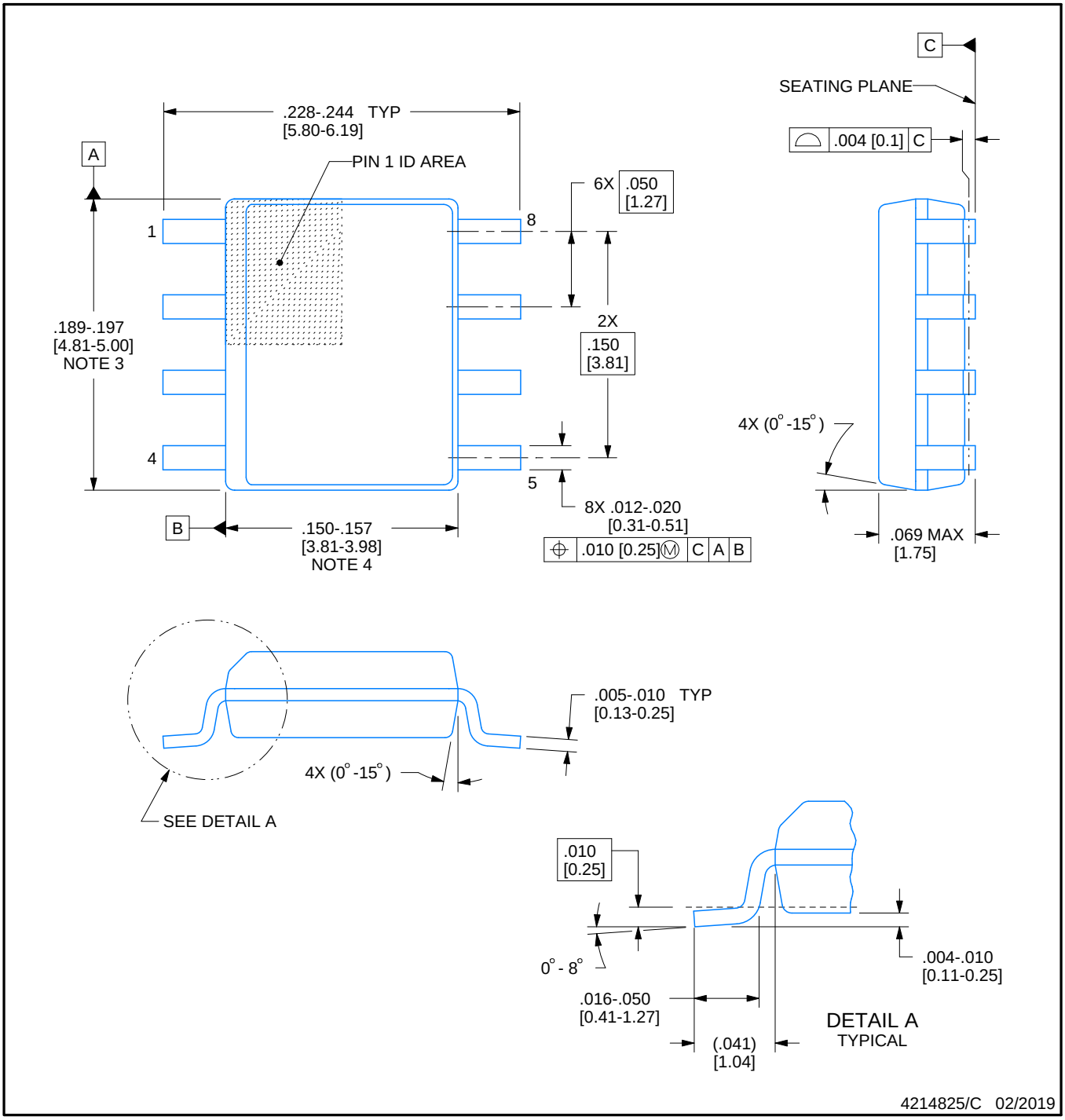
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54232D	D	SOIC	8	75	507	8	3940	4.32

PACKAGE OUTLINE

D0008A

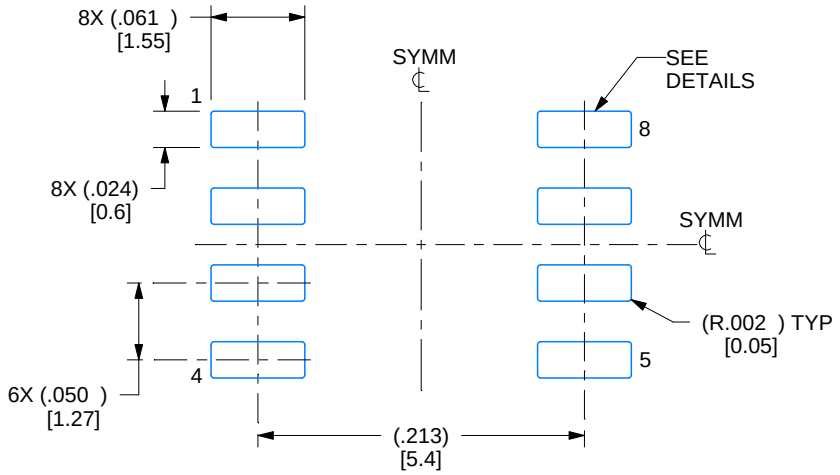
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

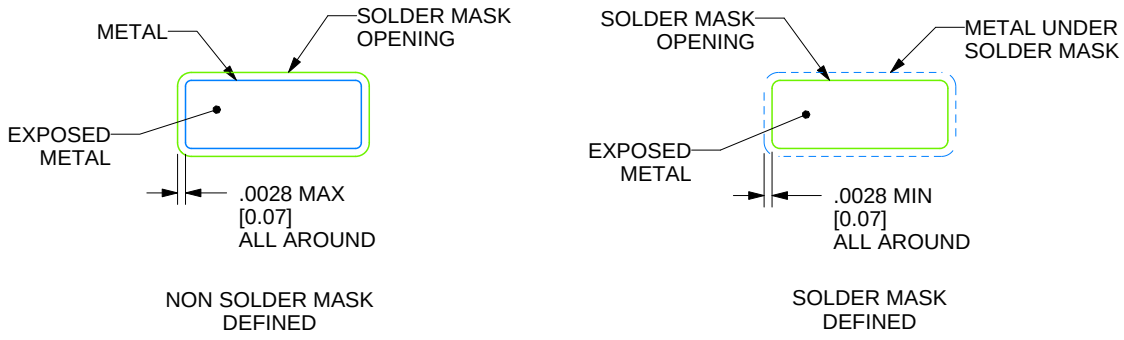


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

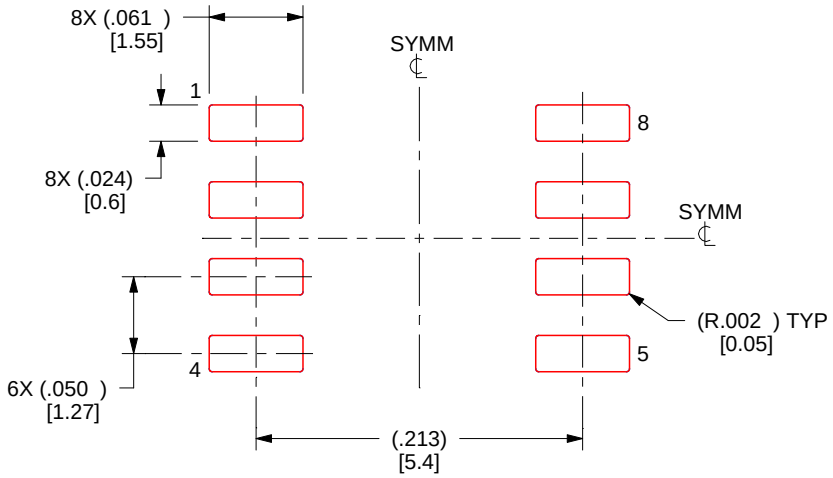
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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