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OPA209AIDR

Texas instruments

Operational Amplifiers - Op Amps 2.2nV/rtHz18MHz PrecRRO36V Op Amp

TEXAS INSTRUMENTS

OPA209, OPA2209, OPA4209

SBOS426D – NOVEMBER 2008 – REVISED OCTOBER 2016

OPAx209 2.2-nV/√Hz, Low-Power, 36-V Operational Amplifier

1 Features

- Low Voltage Noise: 2.2 nV/√Hz at 1 kHz
- 0.1-Hz to 10-Hz Noise: 130 nV_{PP}
- Low Quiescent Current: 2.5 mA/Ch (Maximum)
- Low Offset Voltage: 150 µV (Maximum)
- Gain Bandwidth Product: 18 MHz
- Slew Rate: 6.4 V/µs
- Wide Supply Range:
  ±2.25 V to ±18 V, 4.5 V to 36 V
- Rail-to-Rail Output
- Short-Circuit Current: ±65 mA
- Available in 5-Pin SOT-23, 8-Pin MSOP, 8-Pin SOIC, and 14-Pin TSSOP Packages

2 Applications

- PLL Loop Filters
- Low-Noise, Low-Power Signal Processing
- Low-Noise Instrumentation Amplifiers
- High-Performance ADC Drivers
- High-Performance DAC Output Amplifiers
- Active Filters
- Ultrasound Amplifiers
- Professional Audio Preamplifiers
- Low-Noise Frequency Synthesizers
- Infrared Detector Amplifiers
- Hydrophone Amplifiers

3 Description

The OPA209 series of precision operational amplifiers achieve very low voltage noise density (2.2 nV/√Hz) with a supply current of only 2.5 mA (maximum). This series also offers rail-to-rail output swing, which helps to maximize dynamic range.

In precision data acquisition applications, the OPA209 provides fast settling time to 16-bit accuracy, even for 10-V output swings. This excellent ac performance, combined with only 150 µV (maximum) of offset and low drift over temperature, makes the OPA209 very suitable for fast, high-precision applications.

The OPA209 is specified over a wide dual power-supply range of ±2.25 V to ±18 V, or single-supply operation from 4.5 V to 36 V.

The OPA209 is available in the 5-pin SOT-23, 8-pin VSSOP, and the standard 8-pin SOIC packages. The dual OPA2209 comes in both 8-pin VSSOP and 8-pin SOIC packages. The quad OPA4209 is available in the 14-pin TSSOP package.

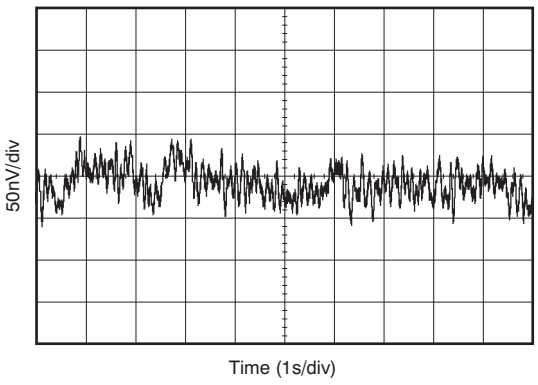
The OPA209 series is specified from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA209	SOT-23 (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA2209	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA4209	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

0.1-Hz to 10-Hz Noise



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2013) to Revision D **Page**

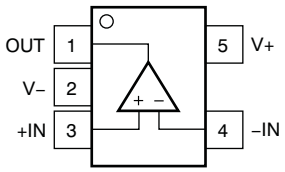
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet ... 1
- Moved specified voltage, specified temperature, and operating temperature from *Electrical Characteristics* to *Recommended Operating Conditions* ... 5
- Updated values in the *Thermal Information* tables to align with JEDEC standards ... 5

Changes from Revision B (August 2010) to Revision C **Page**

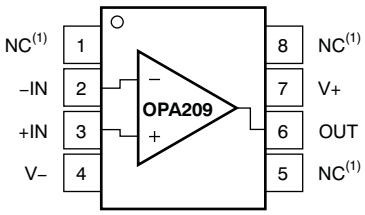
- Deleted device graphic ... 1
- Changed y-axis units label in Figure 2 ... 8

5 Pin Configuration and Functions

OPA209: DBV Package
5-Pin SOT-23
Top View



OPA209: D or DGK Packages
8-Pin SOIC or VSSOP
Top View

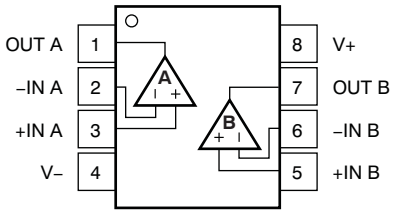


(1) NC = no internal connection

Pin Functions: OPA209

PIN			I/O	DESCRIPTION
NAME	SOT-23	SOIC, VSSOP		
–IN	4	2	I	Inverting input
+IN	3	3	I	Noninverting input
NC	—	1, 5, 8	—	No internal connection
OUT	1	6	O	Output
V–	2	4	—	Negative (lowest) power supply
V+	5	7	—	Positive (highest) power supply

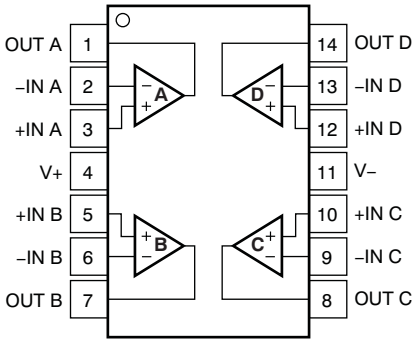
OPA2209: D or DGK Packages
8-Pin SOIC or VSSOP
Top View



Pin Functions: OPA2209

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

OPA4209: PW Package
14-Pin TSSOP
Top View



Pin Functions: OPA4209

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)		40	V
	Signal input pins(2)	(V–) – 0.5	(V+) + 0.5	V
Current	Signal input pins(2)	–10	10	mA
	Output short circuit(3)	Continuous		
Temperature	Operating, T_A	–55	150	°C
	Junction, T_J		200	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For input voltages beyond the power-supply rails, voltage or current must be limited.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Specified voltage	±2.25	±18	V
	Specified temperature	–40	125	°C
T_A	Operating temperature	–55	150	°C

6.4 Thermal Information: OPA209

THERMAL METRIC(1)		OPA209			UNIT
		DBV (SOT-23)	D (SOIC)	DGK (VSSOP)	
		5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.9	135.5	142.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	200	73.7	46.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	113.1	61.9	63.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38.2	19.7	5.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	104.9	54.8	62.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2209

THERMAL METRIC(1)		OPA2209		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.3	132.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.1	38.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.7	52.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	52.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4209

THERMAL METRIC(1)		OPA4209	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

at V_S = ±2.25 V to ±18 V, T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±15 V, V_{CM} = 0 V			±35	±150	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			1	3	µV/°C
PSRR	vs power supply	V_S = ±2.25 V to ±18 V	T_A = 25°C		0.05	0.5	µV/V
			T_A = –40°C to 125°C			1	
	Channel separation	DC (dual and quad versions)			1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0 V	T_A = 25°C		±1	±4.5	nA
			T_A = –40°C to 85°C			±8	
			T_A = –40°C to 125°C			±15	
I_{OS}	Input offset current	V_{CM} = 0 V	T_A = 25°C		±0.7	±4.5	nA
			T_A = –40°C to 85°C			±8	
			T_A = –40°C to 125°C			±15	
NOISE							
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz			0.13		μV_{PP}
	Noise density	f = 10 Hz			3.3		nV/√Hz
		f = 100 Hz			2.25		
		f = 1 kHz			2.2		
I_n	Input current noise density	f = 1 kHz			500		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 1.5		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V, T_A = –40°C to 125°C		120	130		dB

Electrical Characteristics (continued)

at V_S = ±2.25 V to ±18 V, T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT IMPEDANCE							
	Differential				200 || 4		kΩ || pF
	Common-mode				10^9 || 2		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	T_A = 25°C	126	132		dB
			T_A = –40°C to 125°C	120			
		(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 600 Ω(1)	T_A = 25°C	114	120		
			T_A = –40°C to 125°C	110			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				18		MHz
SR	Slew rate				6.4		V/µs
Φm	Phase margin	R_L = 10 kΩ, C_L = 25 pF			80		°
t_S	Settling time	0.1%, G = –1, 10-V step, C_L = 100 pF			2.1		µs
		0.0015% (16-bit), G = –1, 10-V step, C_L = 100 pF			2.6		
	Overload recovery time	G = –1			< 1		µs
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 20 V_{PP}, 600 Ω			0.000025%		
OUTPUT							
	Voltage output swing	R_L = 10 kΩ, A_{OL} > 130 dB		(V–) + 0.2		(V+) – 0.2	V
		R_L = 600 Ω, A_{OL} > 114 dB		(V–) + 0.6		(V+) – 0.6	
		R_L = 10 kΩ, A_{OL} > 120 dB, T_A = –40°C to 125°C		(V–) + 0.2		(V+) – 0.2	
I_{SC}	Short-circuit current	V_S = ±18 V			±65		mA
C_{LOAD}	Capacitive load drive (stable operation)			See *Typical Characteristics*			
Z_O	Open-loop output impedance			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)	I_O = 0 A	T_A = 25°C		2.2	2.5	mA
			T_A = –40°C to 125°C			3.25	

(1) See *Absolute Maximum Ratings* for additional information.

6.8 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

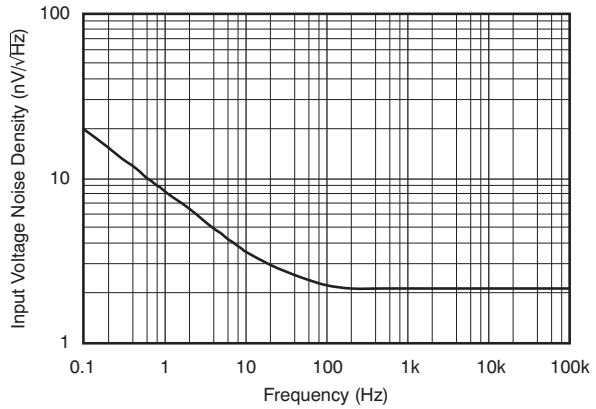


Figure 1. Input Voltage Noise Density vs Frequency

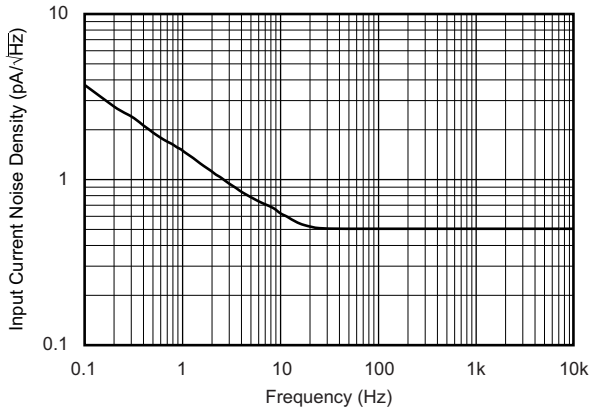


Figure 2. Input Current Noise Density vs Frequency

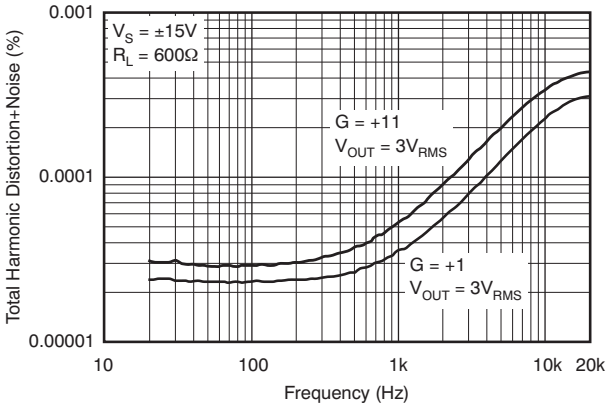


Figure 3. Total Harmonic Distortion + Noise Ratio vs Frequency

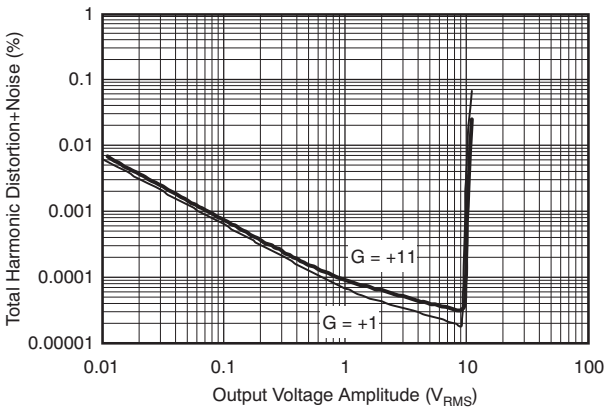


Figure 4. Total Harmonic Distortion + Noise Ratio vs Amplitude

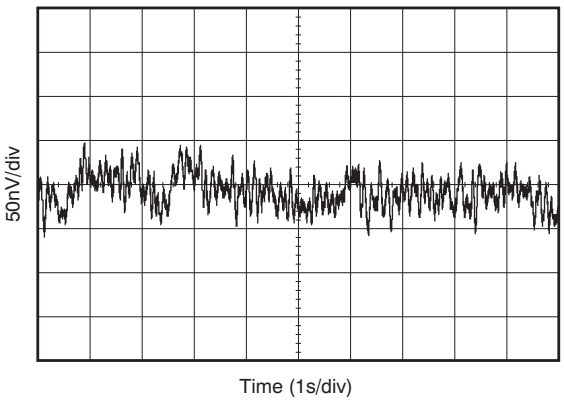


Figure 5. 0.1-Hz to 10-Hz Noise

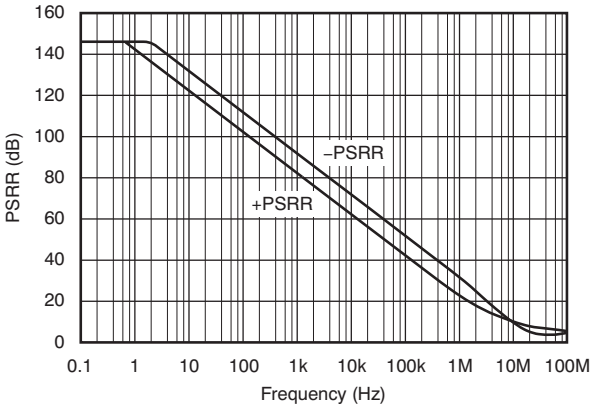


Figure 6. Power-Supply Rejection Ratio vs Frequency (Referred to Input)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

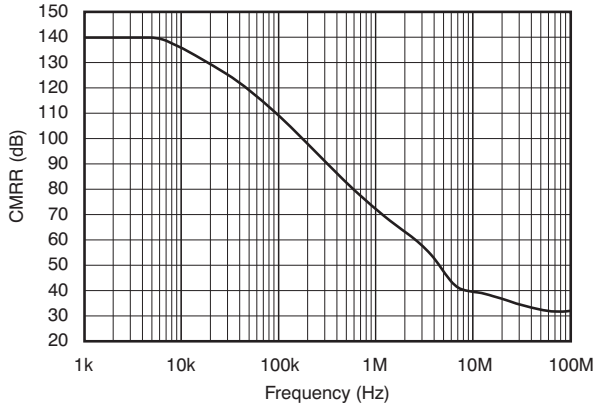


Figure 7. Common-Mode Rejection Ratio vs Frequency

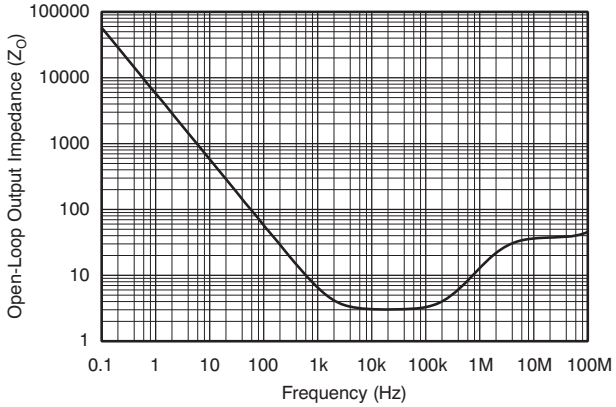


Figure 8. Open-Loop Output Impedance vs Frequency

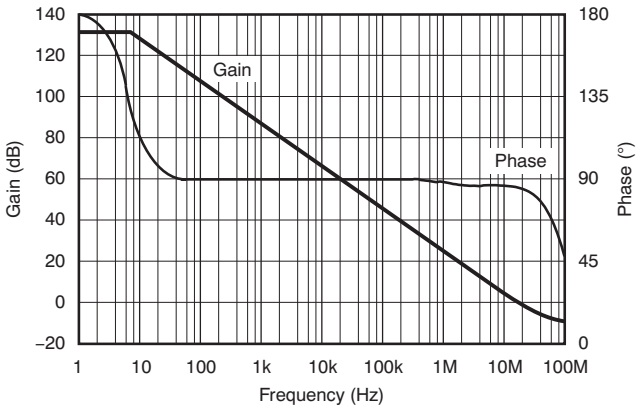


Figure 9. Open-Loop Gain and Phase vs Frequency

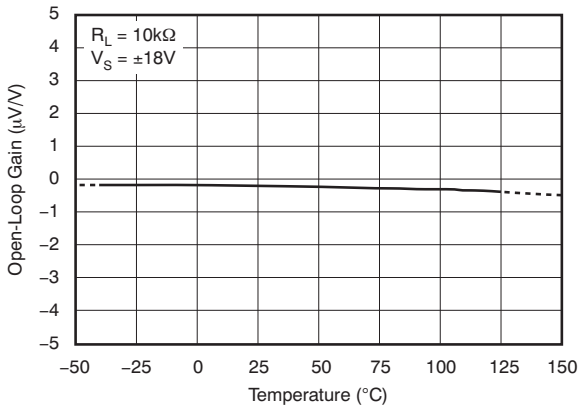


Figure 10. Open-Loop Gain vs Temperature

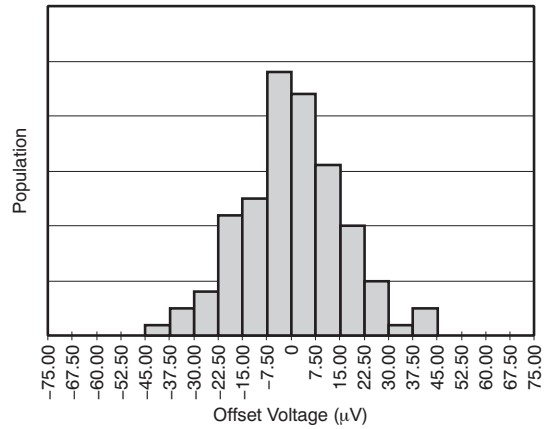


Figure 11. Offset Voltage Production Distribution

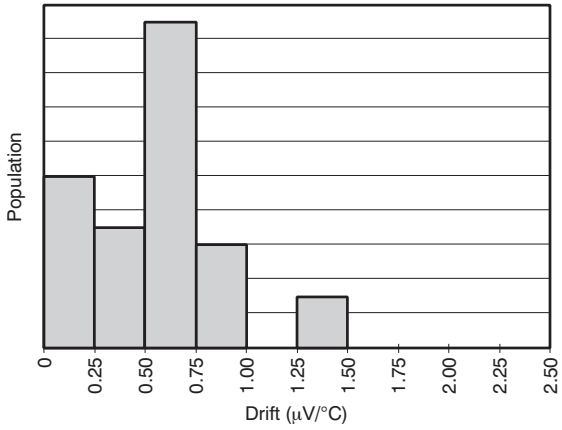


Figure 12. Offset Voltage Drift Production Distribution

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

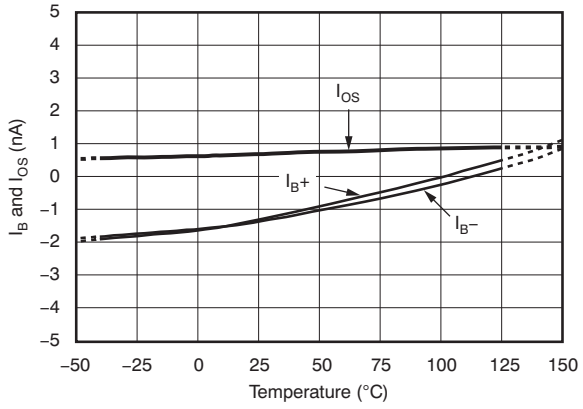


Figure 13. Input Bias and Input Offset Currents vs Temperature

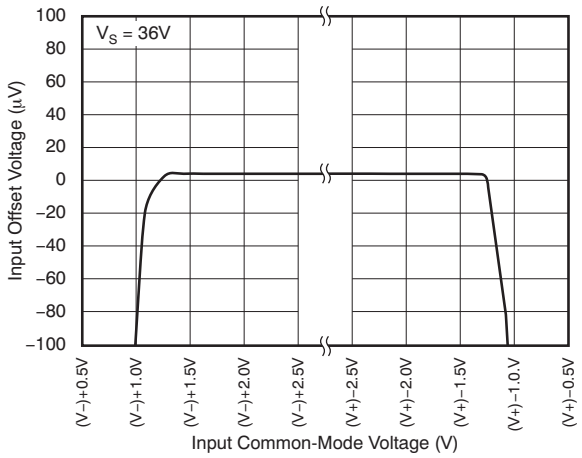


Figure 14. Input Offset Voltage vs Common-Mode Voltage

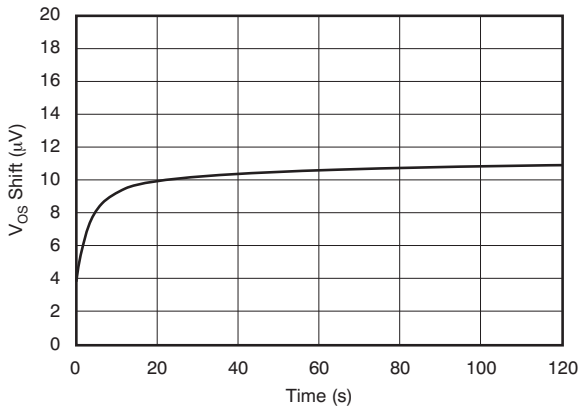


Figure 15. Input Offset Voltage vs Time

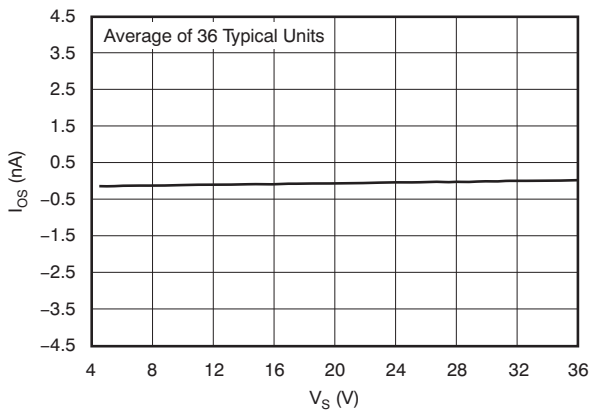


Figure 16. Input Offset Current vs Supply Voltage

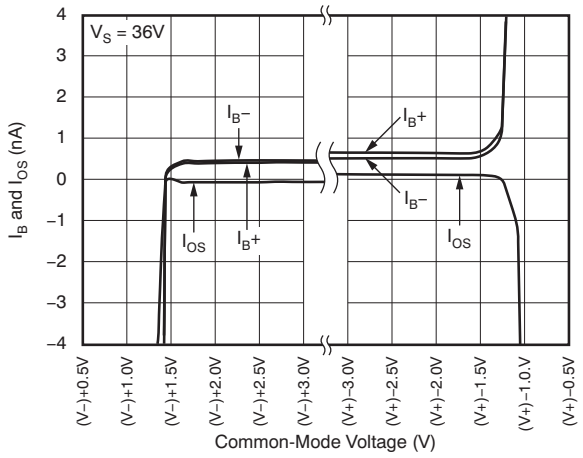


Figure 17. Input Bias and Input Offset Currents vs Common-Mode Voltage

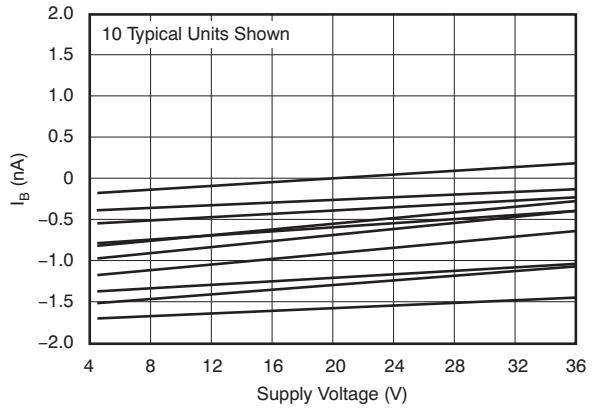


Figure 18. Input Bias Current vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

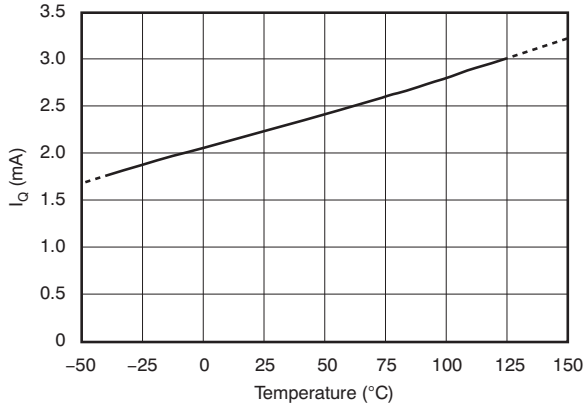


Figure 19. Quiescent Current vs Temperature

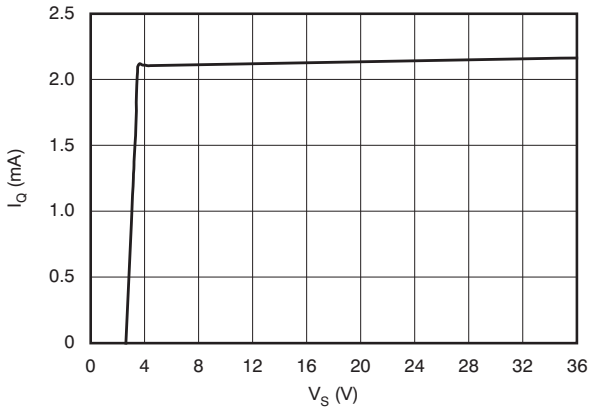


Figure 20. Quiescent Current vs Supply Voltage

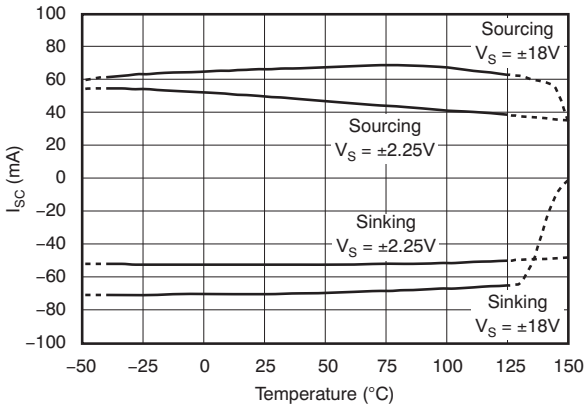


Figure 21. Short-Circuit Current vs Temperature

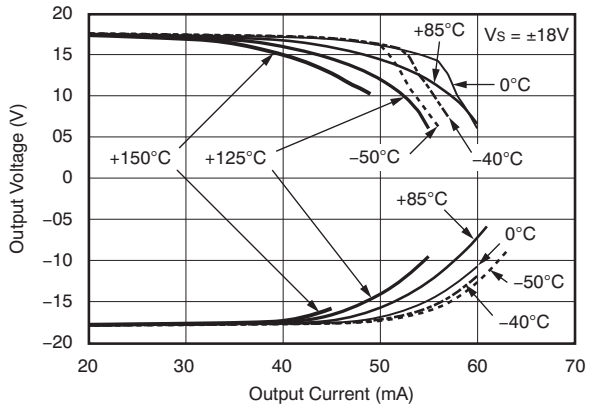


Figure 22. Output Voltage vs Output Current

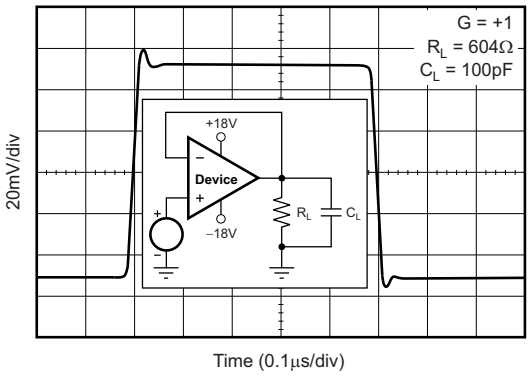


Figure 23. Small-Signal Step Response

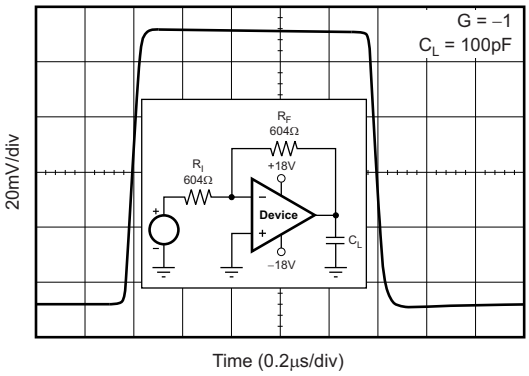


Figure 24. Small-Signal Step Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

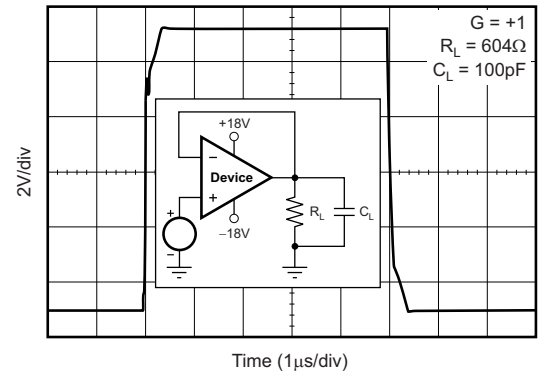


Figure 25. Large-Signal Step Response

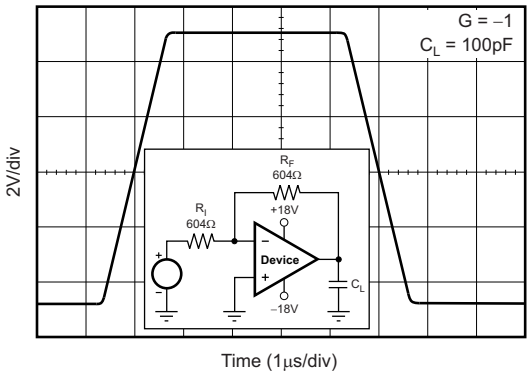


Figure 26. Large-Signal Step Response

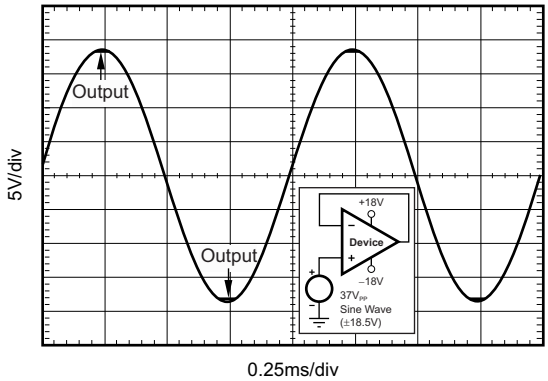


Figure 27. No Phase Reversal

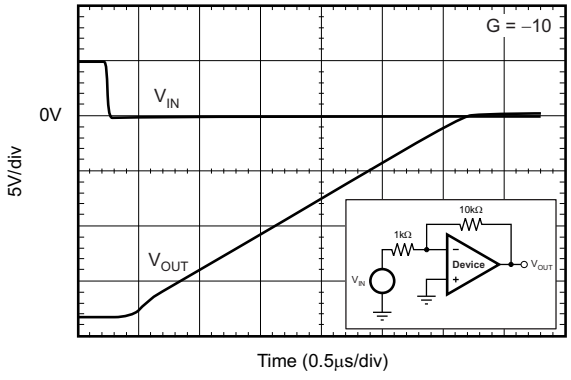


Figure 28. Negative Overload Recovery

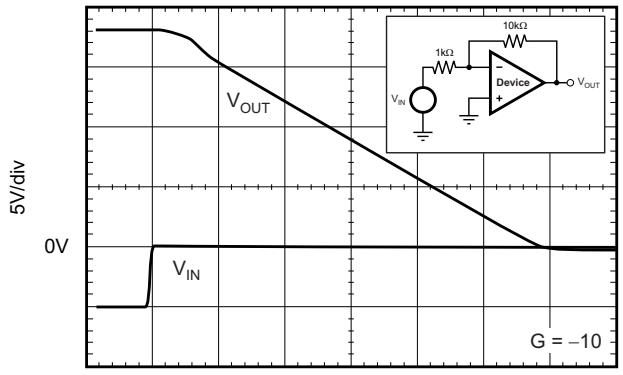


Figure 29. Positive Overvoltage Recovery

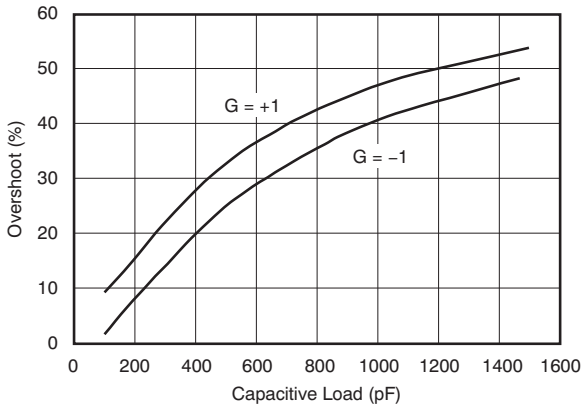


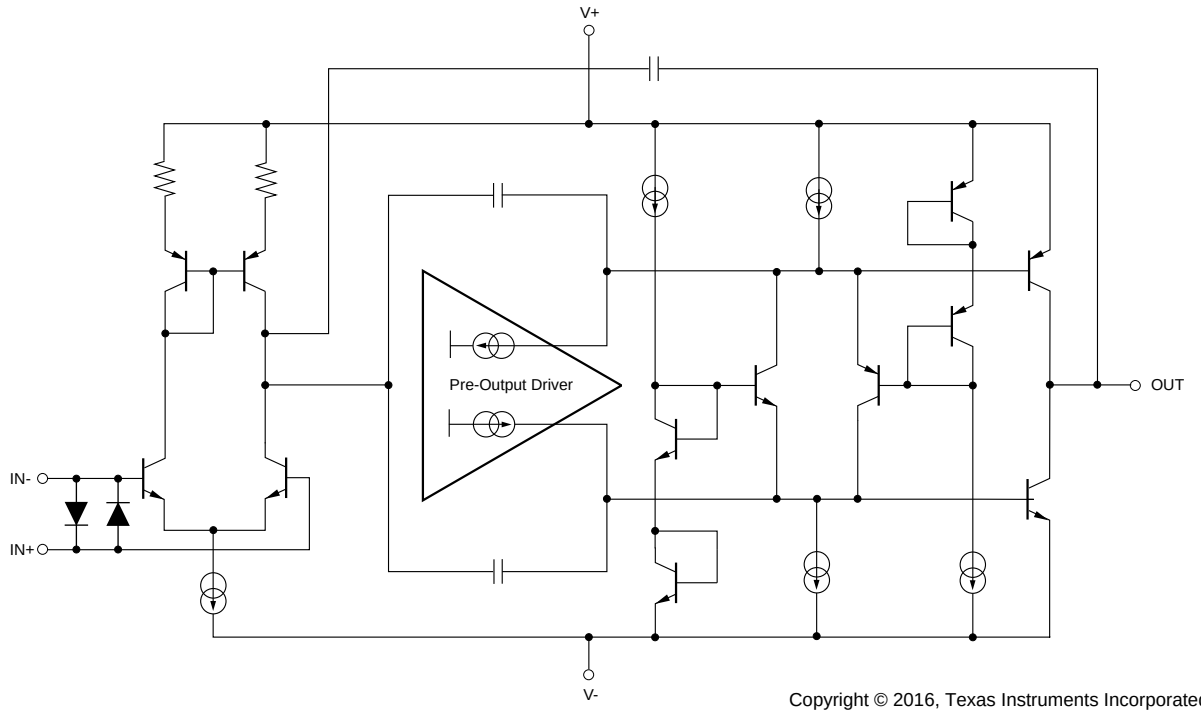
Figure 30. Small-Signal Overshoot vs Capacitive Load

7 Detailed Description

7.1 Overview

The OPA209 series of precision operational amplifiers are unity-gain stable, and free from unexpected output and phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. The *Functional Block Diagram* shows a simplified schematic of the OPA209. This die uses a SiGe bipolar process and contains 180 transistors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA209 series of op amps can be used with single or dual supplies within an operating range of V_S = 4.5 V (±2.25 V) up to 36 V (±18 V). Supply voltages higher than 40 V total can permanently damage the device (see *Absolute Maximum Ratings*).

In addition, key parameters are assured over the specified temperature range, T_A = –40°C to 125°C. Parameters that vary significantly with operating voltage or temperature are shown in the *Typical Characteristics*.

7.3.2 Input Protection

The input terminals of the OPA209 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 31. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 25 and Figure 26 in *Typical Characteristics*. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA209. See *Noise Performance* for further information on noise performance.

Feature Description (continued)

Figure 31 shows an example configuration that implements a current-limiting feedback resistor.

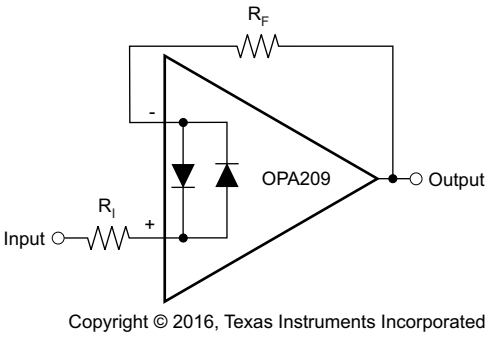


Figure 31. Pulsed Operation

7.3.3 Noise Performance

Figure 32 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with the total circuit noise calculated. The OPA209 has very low voltage noise, making it ideal for low source impedances (less than 2 kΩ). As a comparable precision FET-input op amp (very low current noise), the OPA827 has somewhat higher voltage noise, but lower current noise. It provides excellent noise performance at moderate to high source impedance (10 kΩ and up). For source impedance lower than 300 Ω, the OPA211 may provide lower noise.

The equation in Figure 32 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise,
- i_n = current noise,
- R_S = source impedance,
- k = Boltzmann's constant = 1.38×10^{-23} J/K, and
- T = temperature in Kelvins

For more details on calculating noise, see *Basic Noise Calculations*.

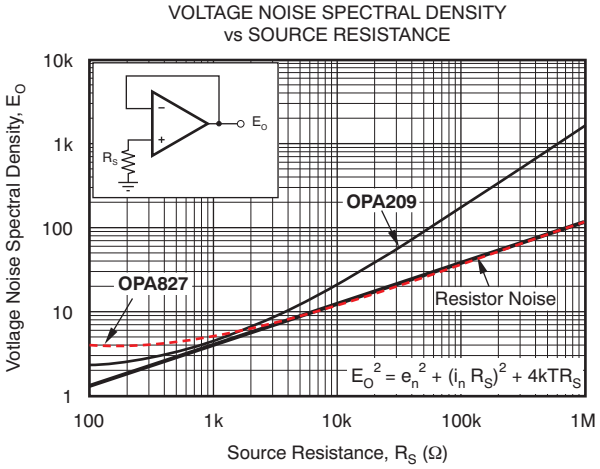


Figure 32. Noise Performance of the OPA209 and OPA827 in Unity-Gain Buffer Configuration

Feature Description (continued)

7.3.4 Basic Noise Calculations

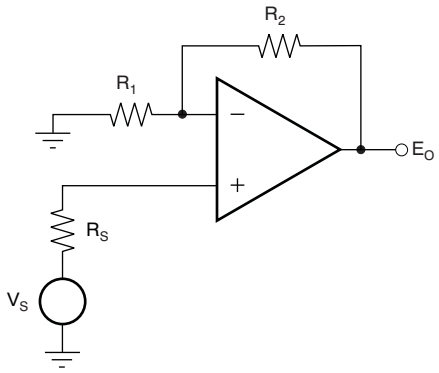
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combinations of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is illustrated in Figure 32. The source impedance is usually fixed; consequently, select the appropriate op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 33 illustrates both noninverting (Figure 33a) and inverting (Figure 33b) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components.

The feedback resistor values can generally be chosen to make these noise sources negligible. Note that low-impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

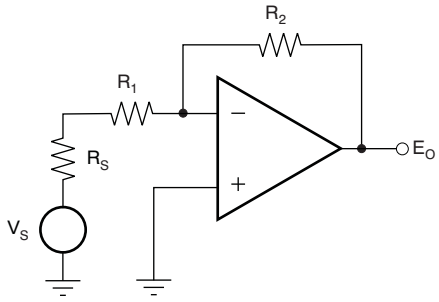
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA209 series op amps at 1 kHz, e_n = 2.2 nV/$\sqrt{Hz}$ and I_n = 530 fA/$\sqrt{Hz}$.

Figure 33. Noise Calculation in Gain Configurations

Feature Description (continued)

7.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See Figure 34 for an illustration of the ESD circuits contained in the OPA209 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA209 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one Figure 34 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 34 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

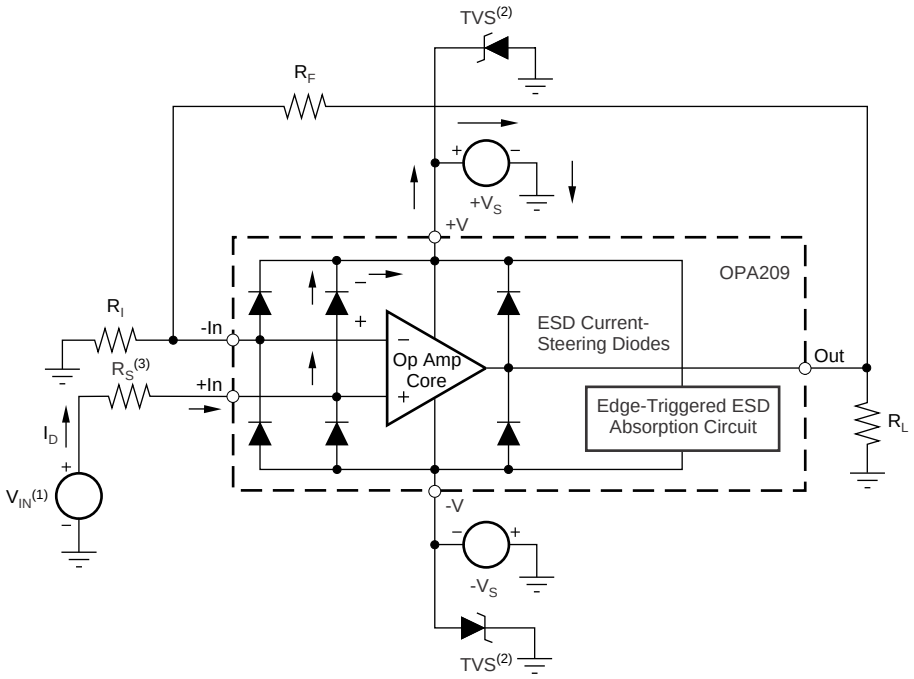
Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0 V.

Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins as shown in Figure 34. The Zener voltage must be selected such that the diode does not turn on during normal operation.

However, its Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

Feature Description (continued)



(1) $V_{IN} = +V_S + 500$ mV

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3) Suggested value approximately 1 kΩ

Figure 34. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

7.4 Device Functional Modes

The OPAx209 is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the OPAx209 is 36 V (±18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx209 are unity-gain stable, precision operational amplifiers with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Typical Application

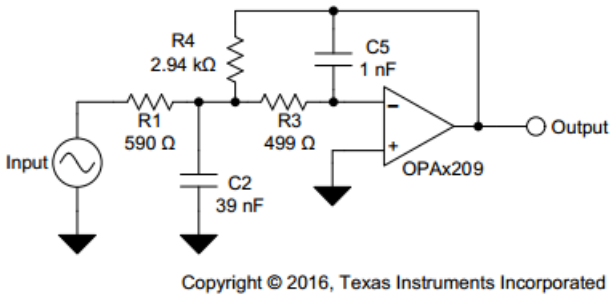


Figure 35. Low-Pass Filter

8.2.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx209 are ideally suited to construct high-speed, high-precision active filters. Figure 35 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 35. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_c = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Typical Application (continued)

8.2.3 Application Curve

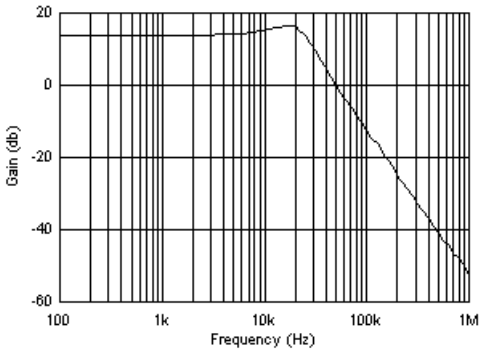


Figure 36. OPAx209 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

9 Power Supply Recommendations

The OPAx209 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

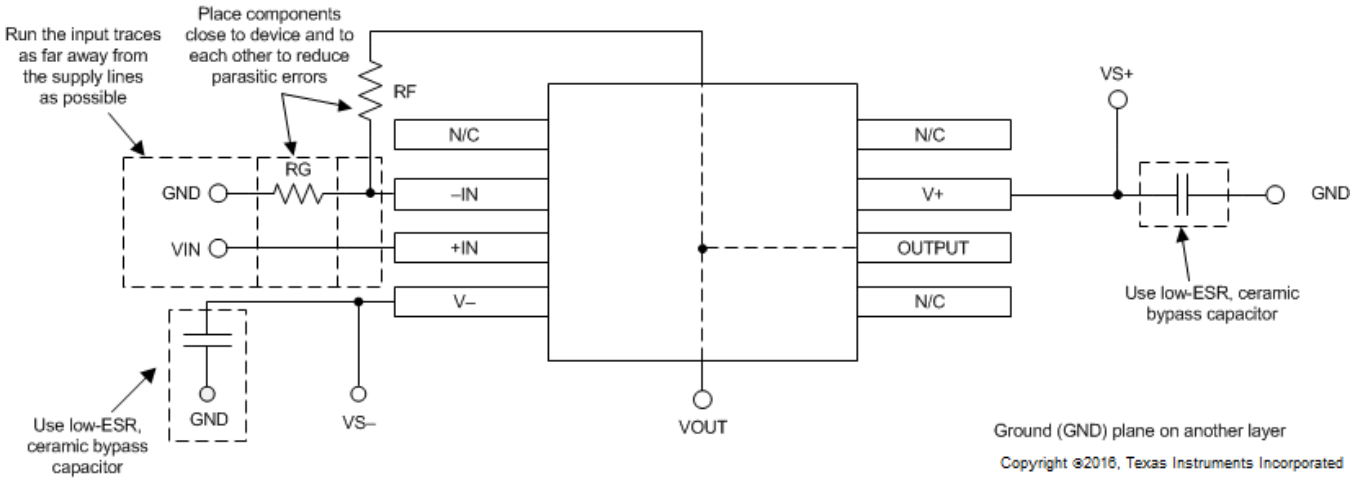


Figure 37. OPAx209 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Operational Amplifier EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP, and SOT-23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the OPAx209 and recommended for reference. All are available for download at www.ti.com (unless otherwise noted):

- *OPA827 Low-Noise, High-Precision, JFET-Input Operational Amplifier* (SBOS376)
- *OPA2x11 1.1-nv/√Hz Noise, Low Power, Precision Operational Amplifier* (SBOS377)
- *OPA209, OPA2209, OPA4209 EMI Immunity Performance* (SBOZ020)
- *Microcontroller PWM to 12-bit Analog Out* (TIDU027)
- *Capacitive Load Drive Solution Using an Isolation Resistor* (TIDU032)
- *Noise Measurement Post Amp* (TIDU016)
- *Diagnostic Patient Monitoring and Therapy Guide* (SLYB147)

11.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA209	Click here	Click here	Click here	Click here	Click here
OPA2209	Click here	Click here	Click here	Click here	Click here
OPA4209	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	O
OPA209AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	
OPA209AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	
OPA209AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	
OPA209AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	
OPA209AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	
OPA209AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	
OPA2209AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	
OPA2209AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	
OPA2209AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	
OPA2209AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	
OPA4209AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	
OPA4209AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including t
do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in sp
reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm
flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

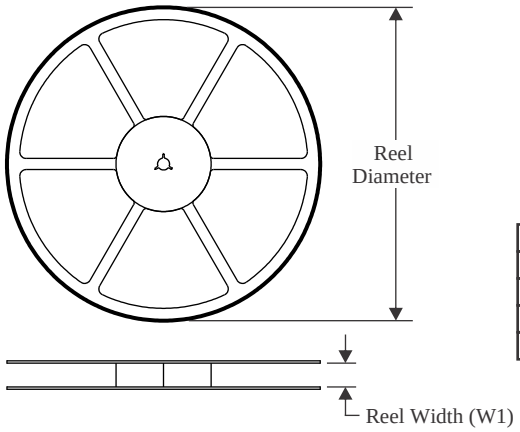
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a li
of the previous line and the two combined represent the entire Device Marking for that device.

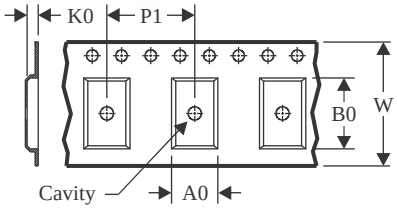
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/B
lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

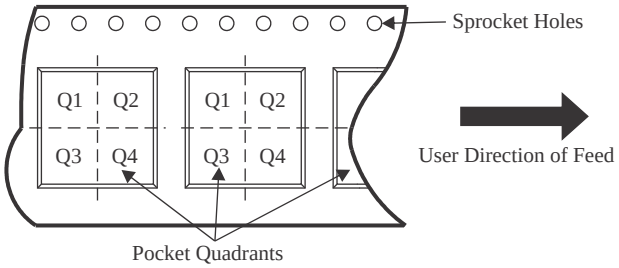


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

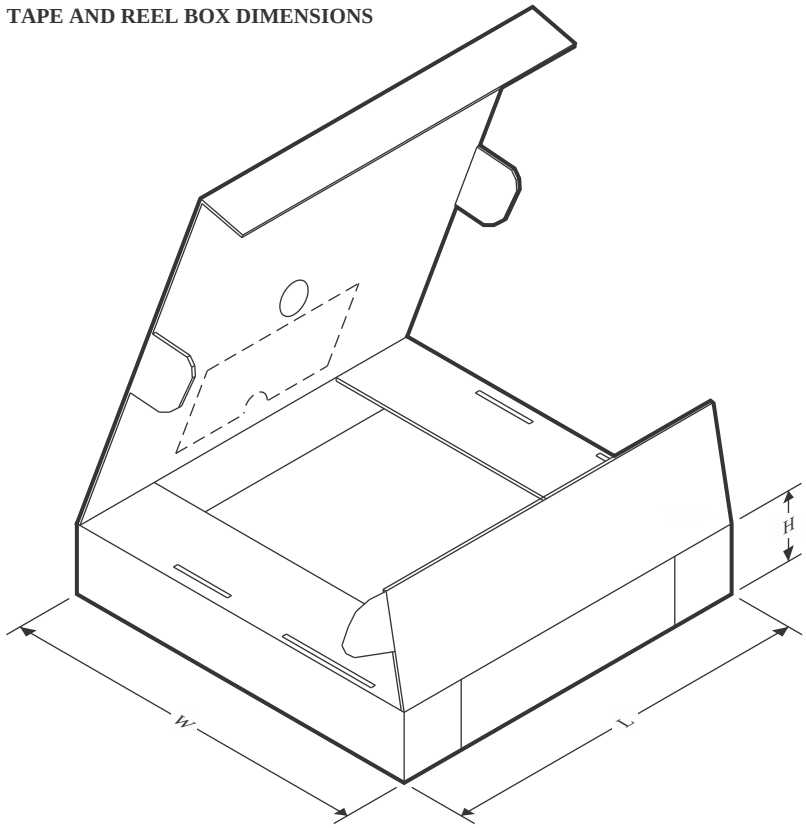
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA209AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA209AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA209AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA209AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA209AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2209AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2209AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2209AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4209AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

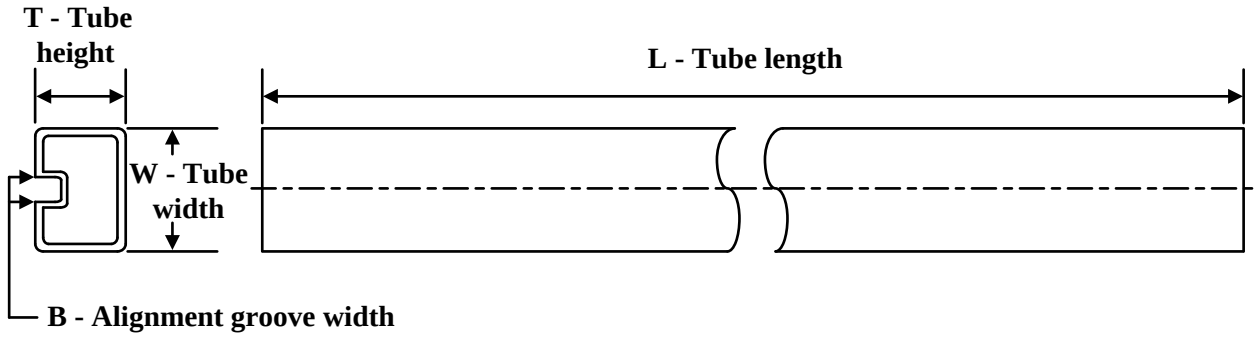
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA209AIDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA209AIDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA209AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA209AIDGKT	VSSOP	DGK	8	250	356.0	356.0	35.0
OPA209AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2209AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2209AIDGKT	VSSOP	DGK	8	250	356.0	356.0	35.0
OPA2209AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4209AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

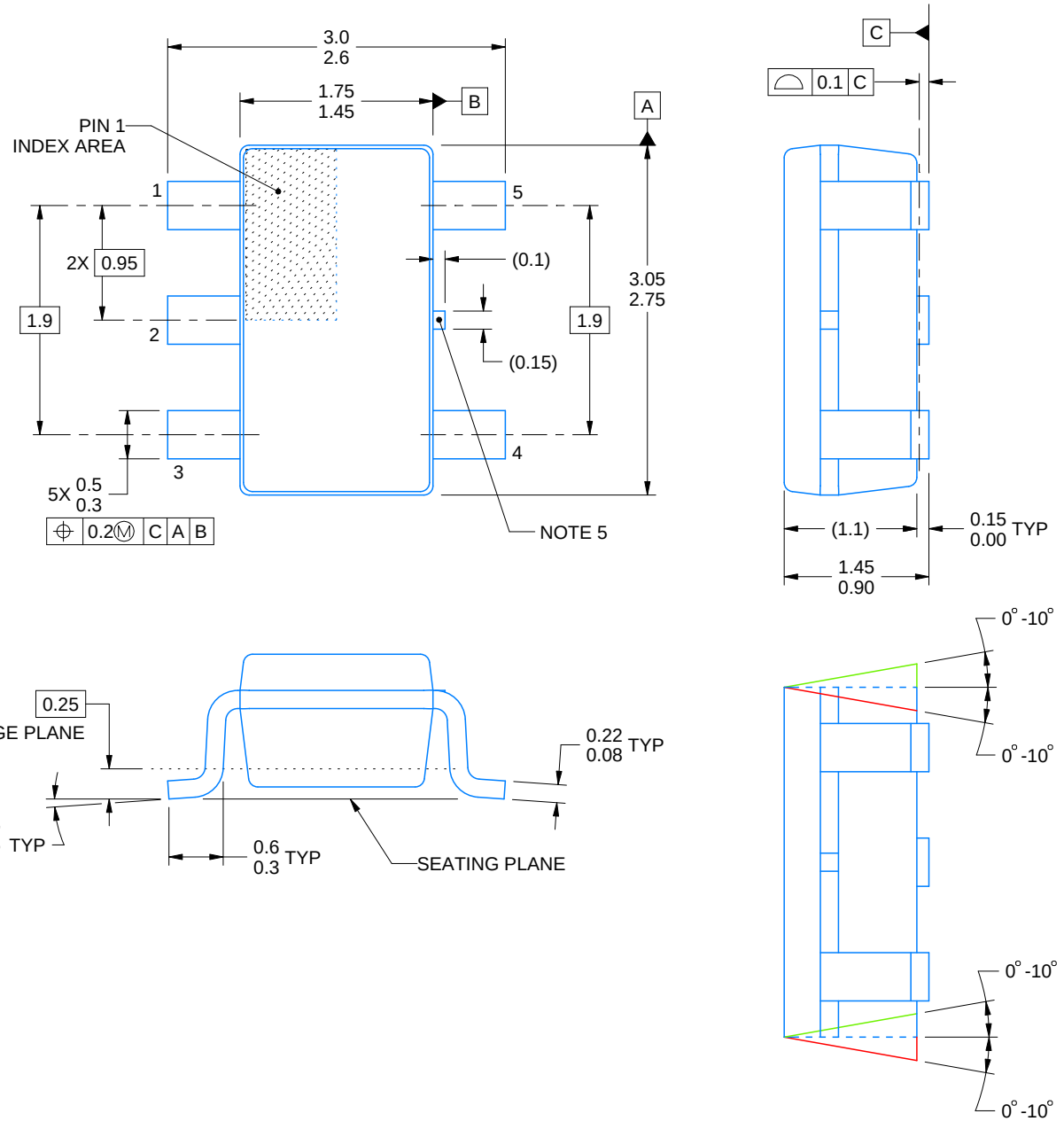
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA209AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2209AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4209AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

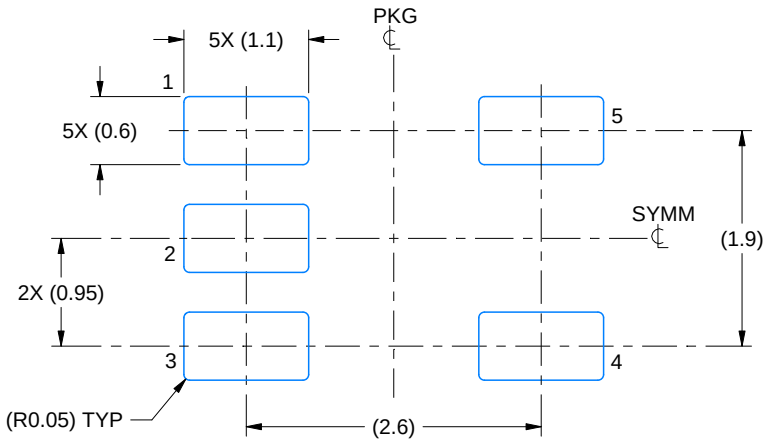


ALTERNATIVE PACKAGE SINGULATION VIEW

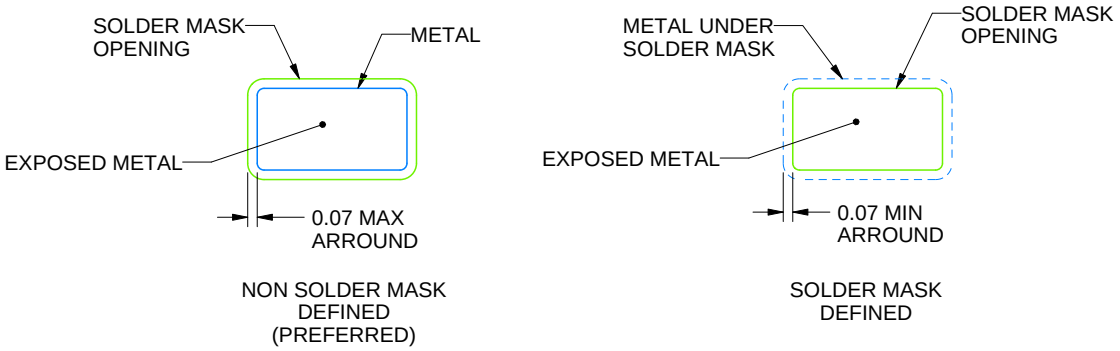
4214839/H 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

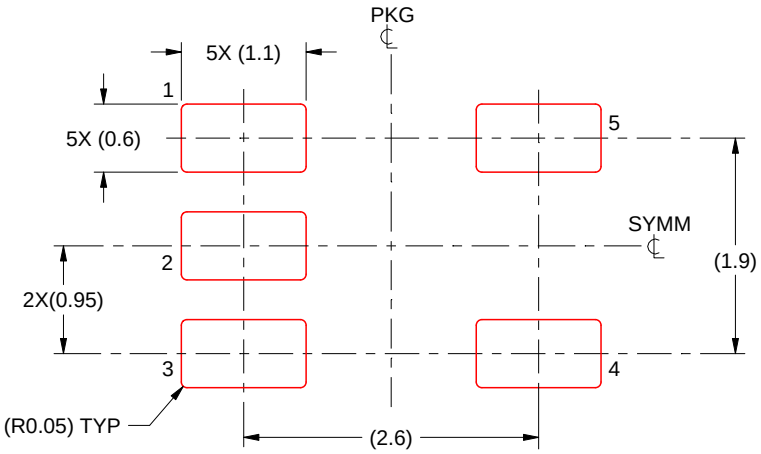


SOLDER MASK DETAILS

4214839/H 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



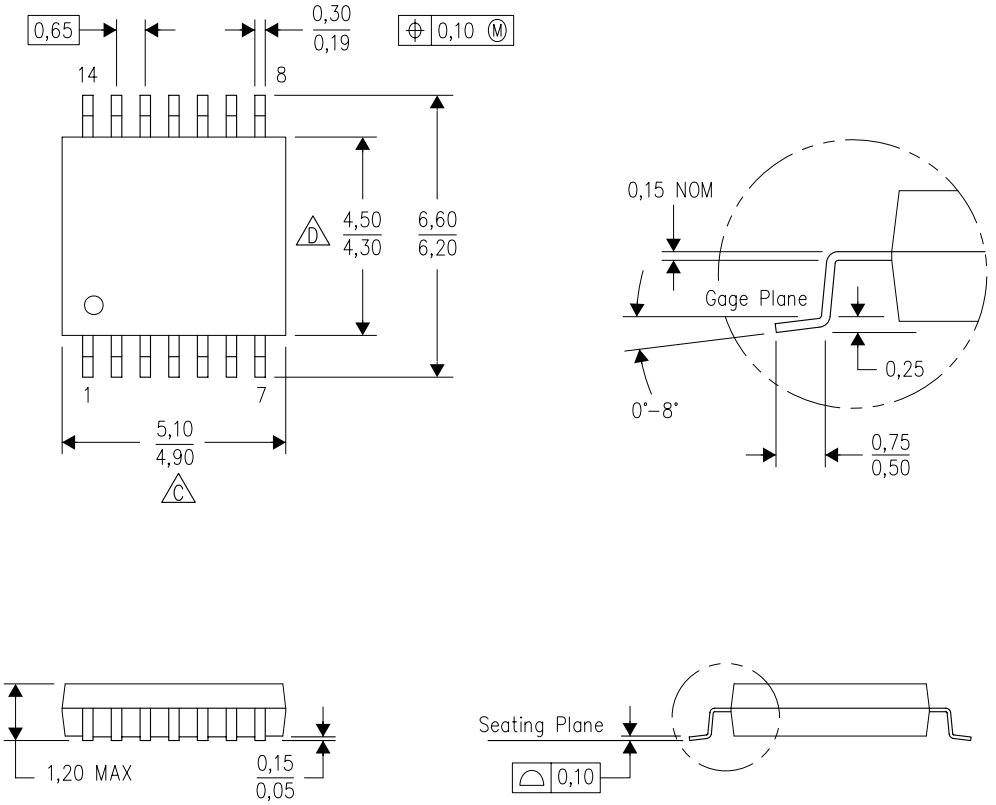
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/H 09/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

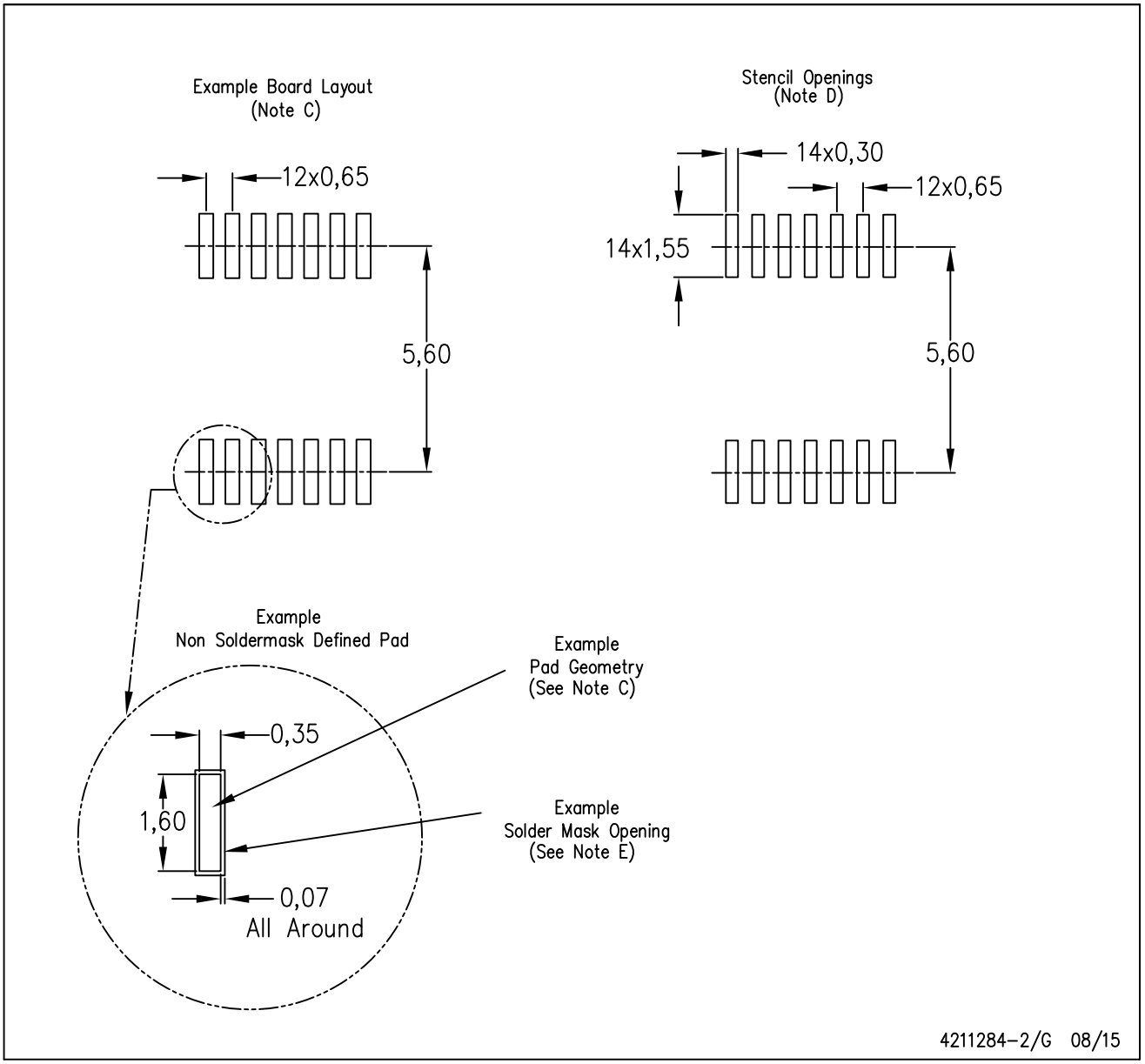
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



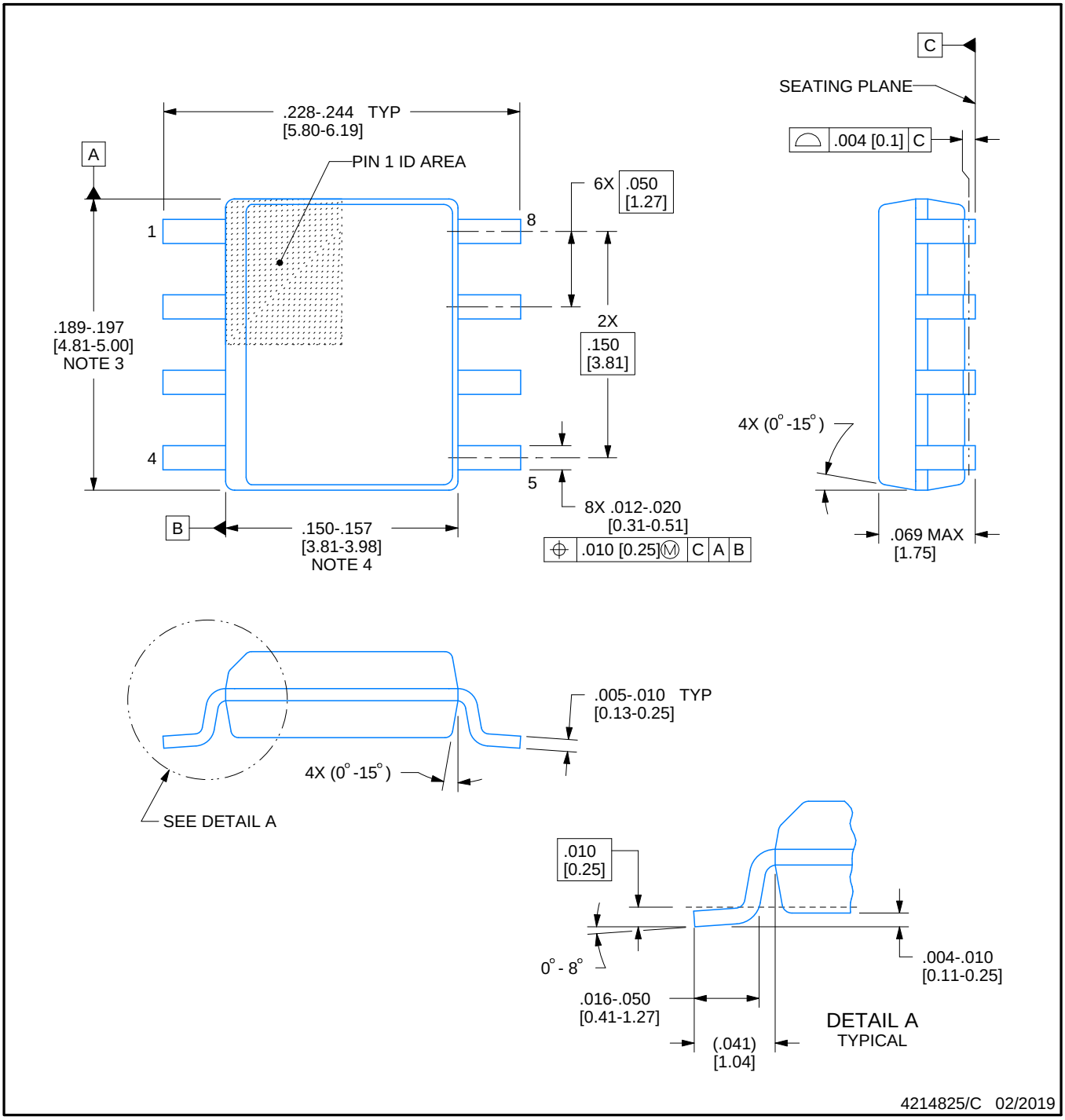
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

D0008A

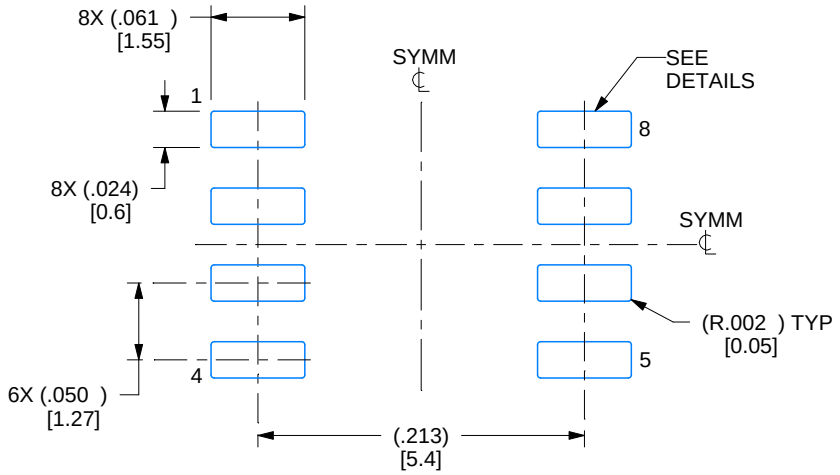
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

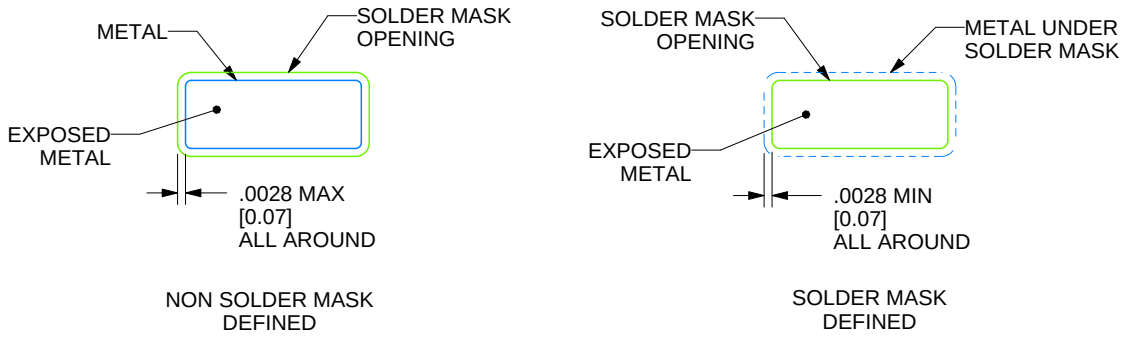


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

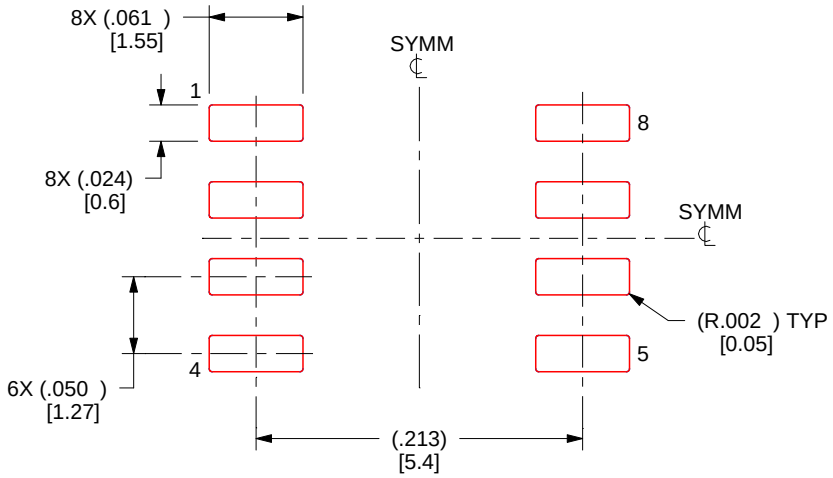
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



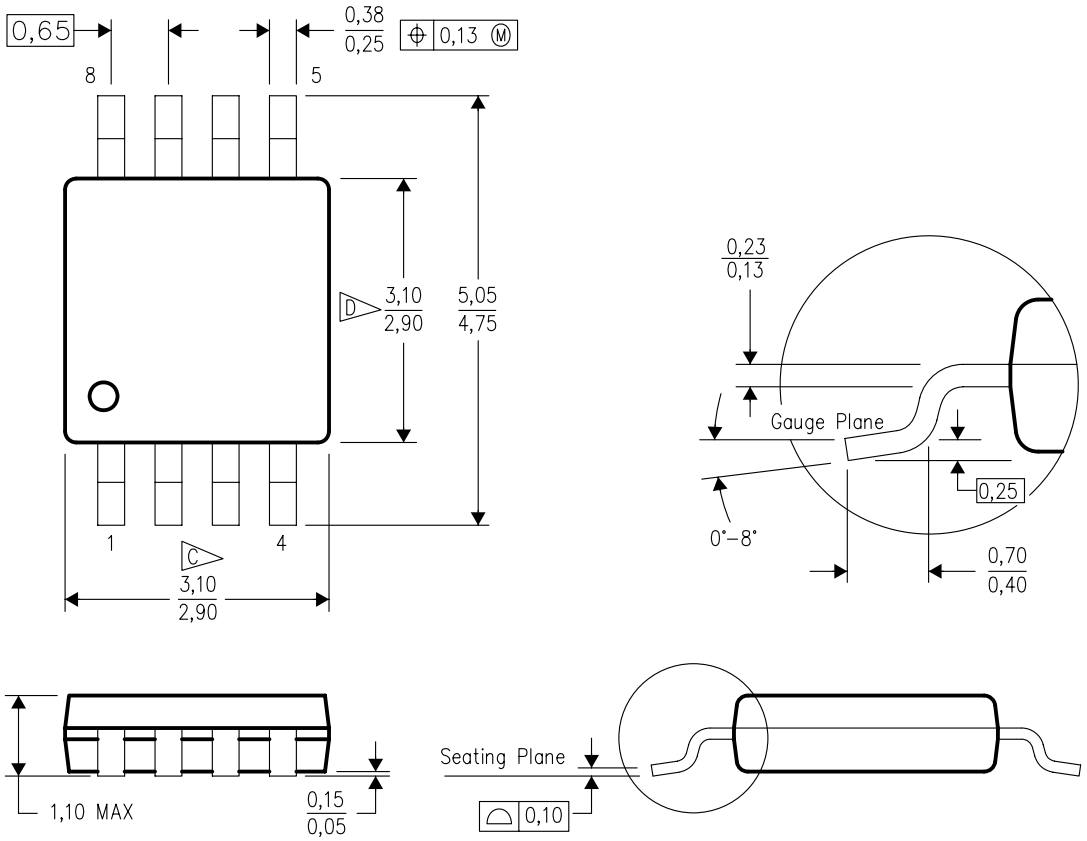
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

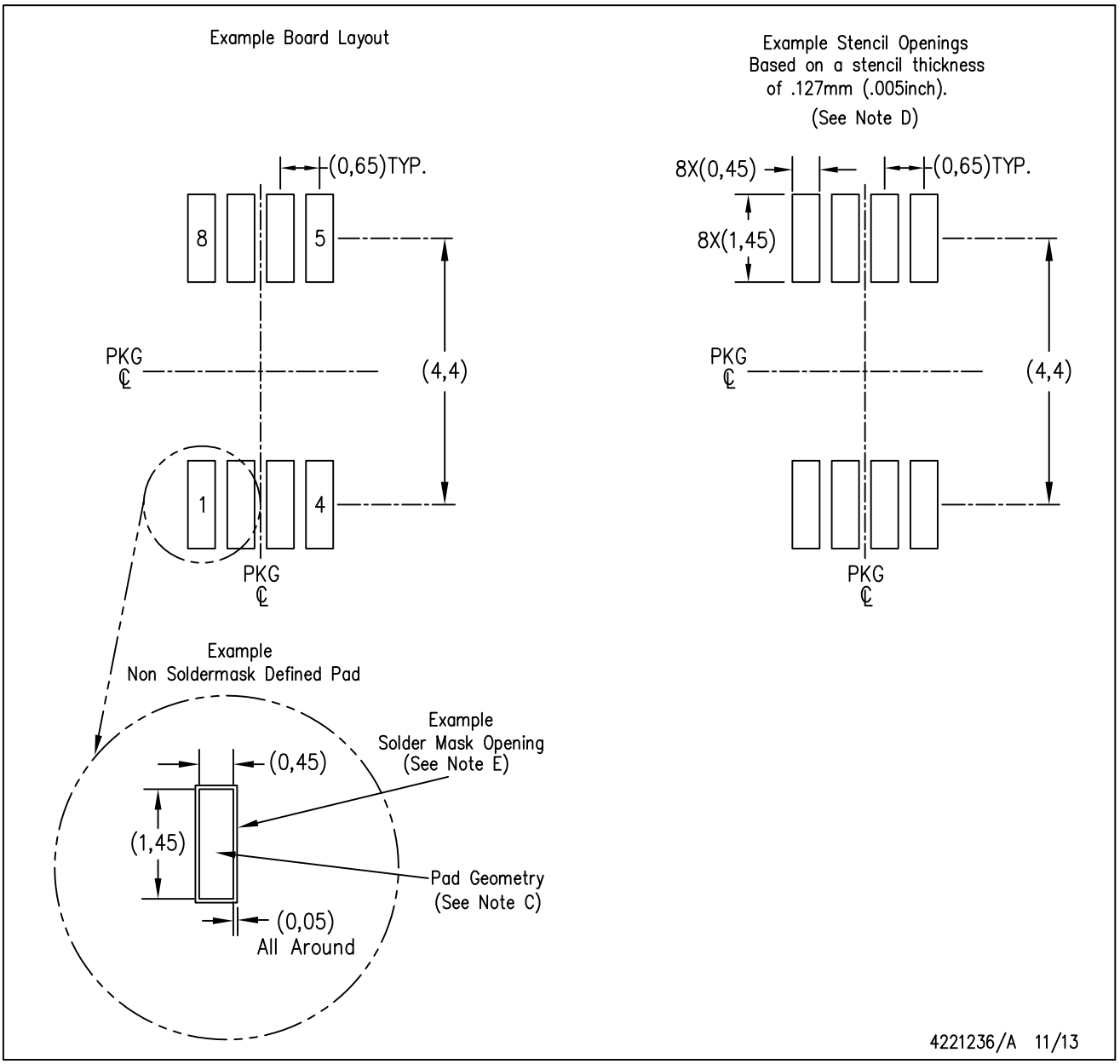
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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