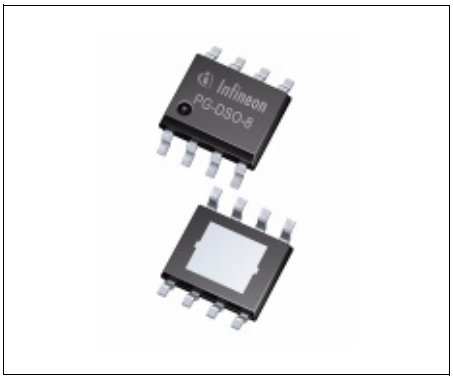
TLE4263-2ES

5-V Low Dropout Voltage Regulator

Automotive Power

Never stop thinking

1 Overview



PG-DSO-8 exposed pad

Features

- Exposed Pad Package with Excellent Thermal Behaviour
- Output Voltage Tolerance ≤ ±2%
- Output Current up to 180 mA
- Very Low Standby Current Consumption
- Watchdog for Monitoring a Microprocessor
- Power-on and Undervoltage Reset with Programmable Delay Time
- Reset Low down to V_Q = 1 V
- Adjustable Reset Threshold
- Very Low Dropout Voltage
- Output Current Limitation
- Reverse Polarity Protection
- Overtemperature Protection
- Wide Temperature Range from -40 °C up to 150 °C
- Input Voltage Range from -42 V to 45 V
- Suitable for Use in Automotive Electronics
- Green Product (RoHS compliant)
- AEC Qualified

Description

TLE4263-2ES is a monolithic integrated very low dropout voltage regulator in a SMD package PG-DSO-8 exposed pad, especially designed for automotive applications. An input voltage up to 45 V is regulated to an output voltage of 5.0 V. The component is able to drive loads up to 180 mA. The IC is short-circuit proof by the implemented current limitation and has an integrated overtemperature shutdown.

It additionally provides features like power-on and undervoltage reset with adjustable reset threshold, a watchdog circuit for monitoring a connected microcontroller and an inhibit input for enabling or disabling the component.

The reset output RO is set to “low” in case the output voltage falls below the reset switching threshold $V_{Q,rt}$. This threshold can be decreased down to 3.5 V by an external resistor divider. The power-on reset delay time can be programmed by the external delay capacitor C_D.

The watchdog circuit provides a monitoring function for microcontrollers: At missing pulses on the watchdog’s input W the reset output RO is set to “low”. The trigger time for the watchdog pulses can be set by the external capacitor C_D.

The IC can be switched off by the inhibit input, reducing the current consumption to typically 0 µA.

Type	Package	Marking
TLE4263-2ES	PG-DSO-8 exposed pad	4263-2

Dimensioning Information on External Components

The input capacitor C_I is recommended for compensation of line influences. The output capacitor C_Q is necessary for the stability of the control loop. Stability is guaranteed at values $\geq 22\ \mu F$ and an ESR of $\leq 3\ \Omega$ within the operating temperature range. For small tolerances of the reset delay the capacitance's spread of the delay capacitor C_D and its temperature coefficient should be taken into consideration.

Circuit Description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The component also has a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

In case the externally scaled down output voltage at the reset adjust input falls below 1.35 V, the external reset delay capacitor C_D is discharged by the reset generator. When the voltage of the capacitor reaches the lower threshold V_{DRL}, a reset signal occurs at the reset output and is held until the upper threshold V_{DU} is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of typically 4.65 V.

2 Block Diagram

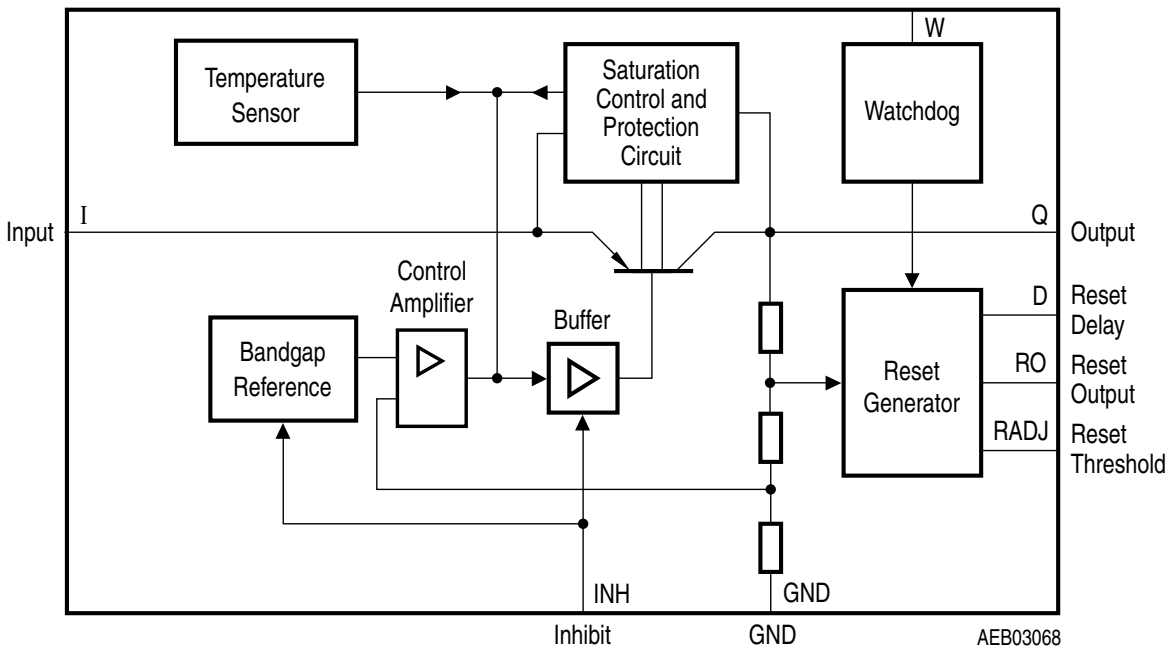


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

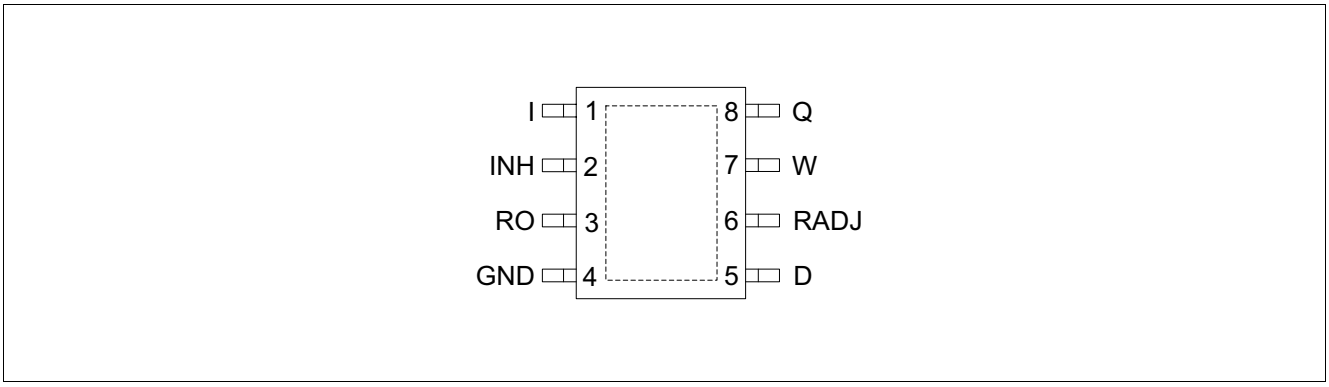


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	I	**Input** for compensating line influences, a capacitor to GND close to the IC terminals is recommended
2	INH	**Inhibit** enables/disables the device; connect to I if the this function is not needed
3	RO	**Reset Output** open-collector output connected to the output via an internal 30kΩ pull-up resistor; leave open if the this function is not needed
4	GND	**Ground**
5	D	**Reset Delay Timing** connect a ceramic capacitor to GND for adjusting the reset delay time / watchdog trigger time; leave open if this function is not needed
6	RADJ	**Reset Threshold Adjust** connect an external voltage divider to adjust the reset switching threshold; connect to GND for using internal threshold
7	W	**Watchdog** rising edge triggered input for monitoring a microcontroller; connect to GND if this function is not needed
8	Q	**Output** block to ground with a capacitor close to the IC terminals with a capacitance value $C \geq 22\ \mu F$, and an $ESR \leq 3\ \Omega$
PAD	–	**Exposed Pad** attach the exposed pad on package bottom to the heatsink area on circuit board; connect to GND

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Input I, Input INH						
4.1.1	Input Voltage	V_I, V_{INH}	-42	45	V	–
Reset Output RO, Reset Delay D						
4.1.2	Voltage	V_R, V_D	-0.3	42	V	–
Reset Threshold RADJ						
4.1.3	Voltage	V_{RADJ}	-0.3	6	V	–
Output Q						
4.1.4	Voltage	V_Q	-0.3	7	V	–
Watchdog W						
4.1.5	Voltage	V_W	-0.3	6	V	–
Temperature						
4.1.6	Junction Temperature	T_j	–	150	°C	–
4.1.7	Storage Temperature	T_{stg}	-50	150	°C	–
ESD Susceptibility						
4.1.8	Human Body Model (HBM)[2)]	Voltage	-	2	kV	–
4.1.9	Charged Device Model (CDM)[3)]	Voltage	-	1	kV	–

1) not subject to production test, specified by design

2) ESD HBM Test according JEDEC JESD22-A114

3) ESD CDM Test according AEC/ESDA ESD-STM5.3.1-1999

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input Voltage	V_I	5.5	45	V	–
4.2.2	Junction Temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1)]	R_{thJC}	–	10	–	K/W	measured to exposed pad
4.3.2	Junction to Ambient[1)]	R_{thJA}	–	45	–	K/W	[2)]
4.3.3		R_{thJA}	–	153	–	K/W	footprint only[3)]
4.3.4		R_{thJA}	–	64	–	K/W	300 mm² heatsink area[3)]
4.3.5		R_{thJA}	–	55	–	K/W	600 mm² heatsink area[3)]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

5 Electrical Characteristics

5.1 Voltage Regulator

Electrical Characteristics Voltage Regulator

V_I = 13.5 V, -40 °C ≤ T_j ≤150 °C, V_{INH} > 3.6 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

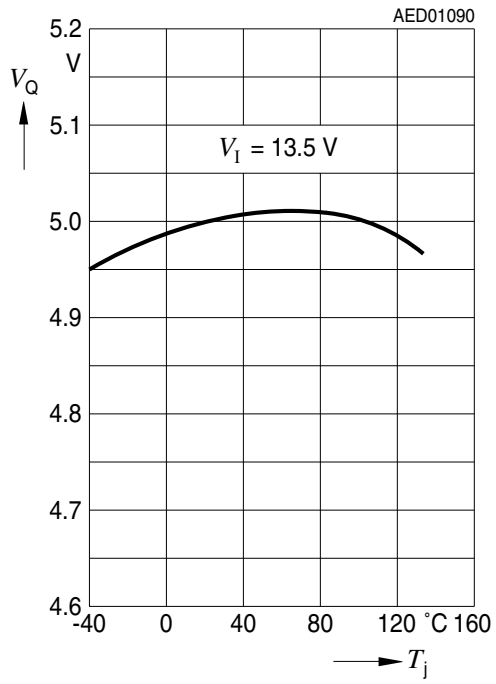
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Output Voltage	V_Q	4.90	5.00	5.10	V	5 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 28 V
5.1.2	Output Voltage	V_Q	4.90	5.00	5.10	V	6 V ≤ V_I ≤ 32 V; I_Q = 100 mA; T_j = 100 °C
5.1.3	Output Current Limitation	$I_{Q,max}$	180	250	400	mA	V_Q = 4.8 V
5.1.4	Dropout voltage	V_{dr}	–	0.35	0.60	V	I_Q = 150 mA[1)]
5.1.5	Load regulation	$\Delta V_{Q,lo}$	–	–	25	mV	I_Q = 5 mA to 150 mA
5.1.6	Line regulation	$\Delta V_{Q.li}$	–	3	25	mV	V_I = 6 V to 28 V; I_Q = 150 mA
5.1.7	Power Supply Ripple Rejection[2)]	$PSRR$	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp

1) Drop voltage = V_i - V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 6 V input).

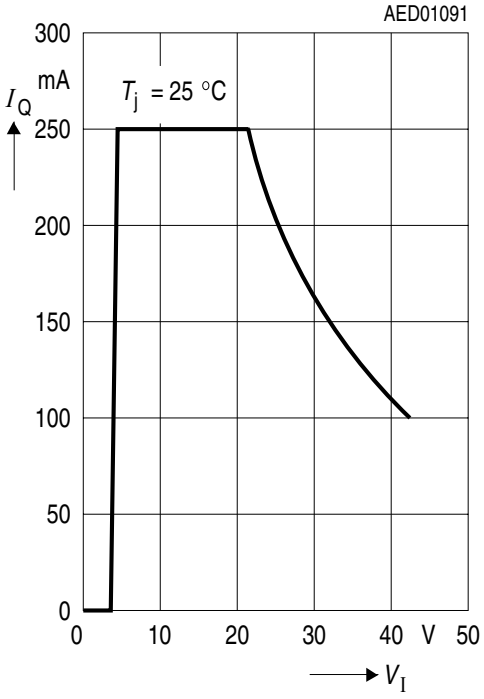
2) Not subject to production test, specified by design.

5.2 Typical Performance Characteristics Voltage Regulator

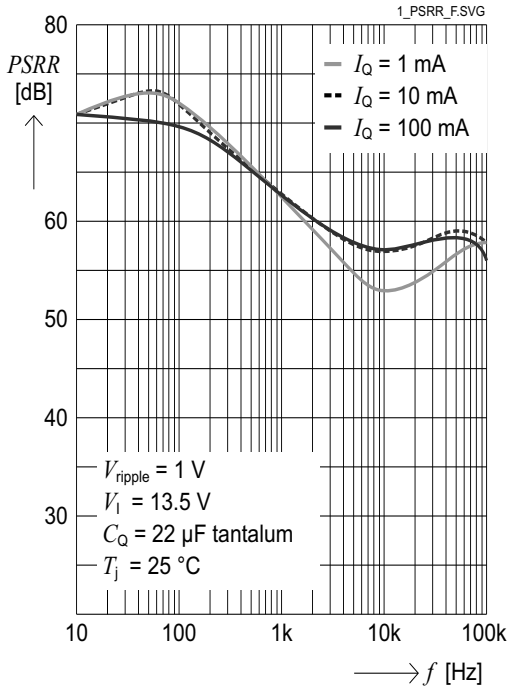
Output Voltage V_Q versus Junction Temperature T_J



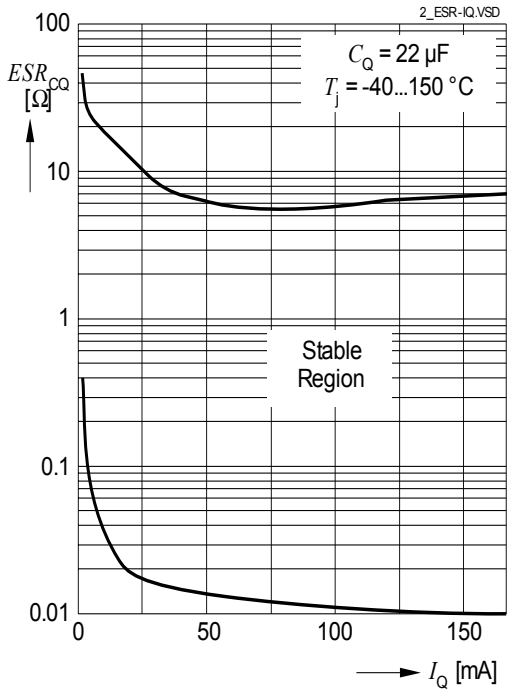
Output Current I_Q versus Input Voltage V_I



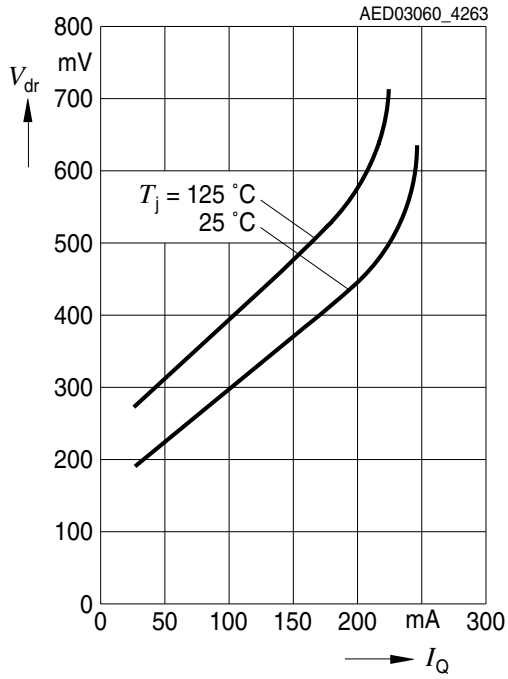
Power Supply Ripple Rejection $PSRR$ versus ripple frequency f_r



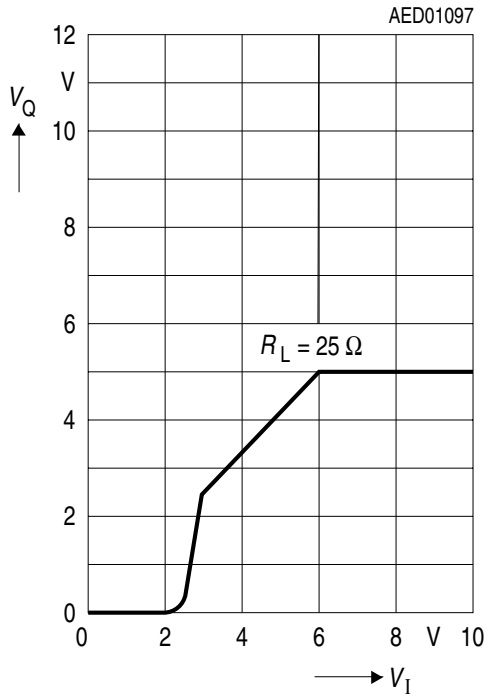
Output Capacitor Series Resistor $ESR(C_Q)$ versus Output Current I_Q



Dropout Voltage V_{dr} versus Output Current I_Q



Output Voltage V_Q versus Input Voltage V_I



5.3 Current Consumption

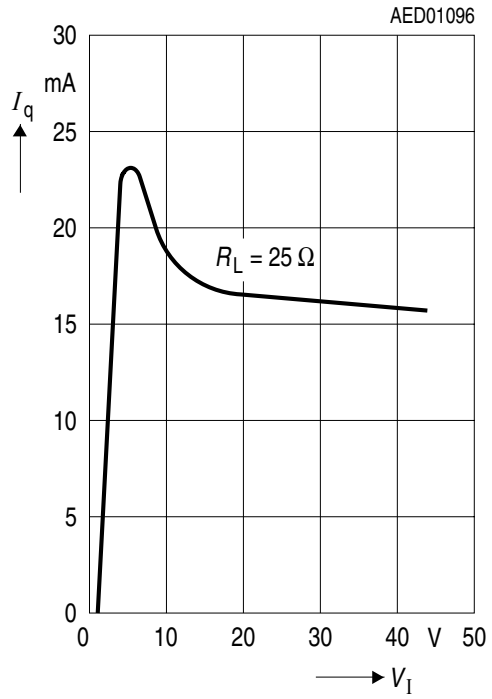
Electrical Characteristics Voltage Regulator

V_I = 13.5 V, -40 °C ≤ T_j ≤150 °C, V_{INH} > 3.6 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

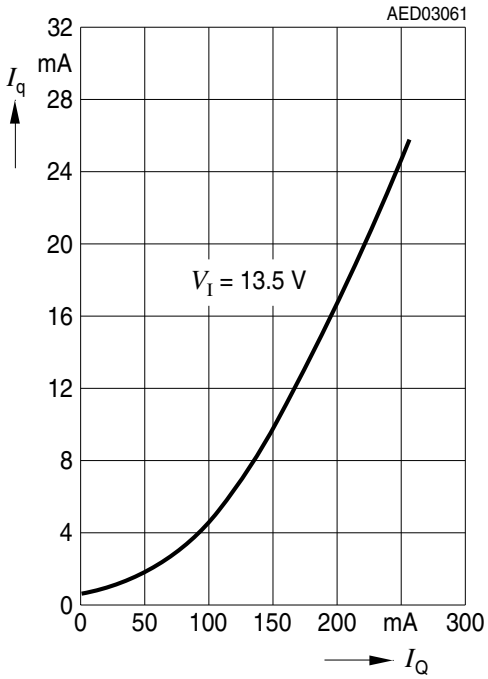
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	Current Consumption; $I_q = I_I - I_Q$	I_q	–	0	10	µA	V_{INH} = 0 V; T_j ≤ 115 °C
5.3.2			–	900	1300	µA	I_Q = 0 mA
5.3.3			–	10	18	mA	I_Q = 150 mA
5.3.4			–	15	24	mA	I_Q = 150 mA; V_I = 4.5 V

5.4 Typical Performance Characteristics Current Consumption

Current Consumption I_q versus Input Voltage V_I



Current Consumption I_q versus Output Current I_Q



5.5 Inhibit Function

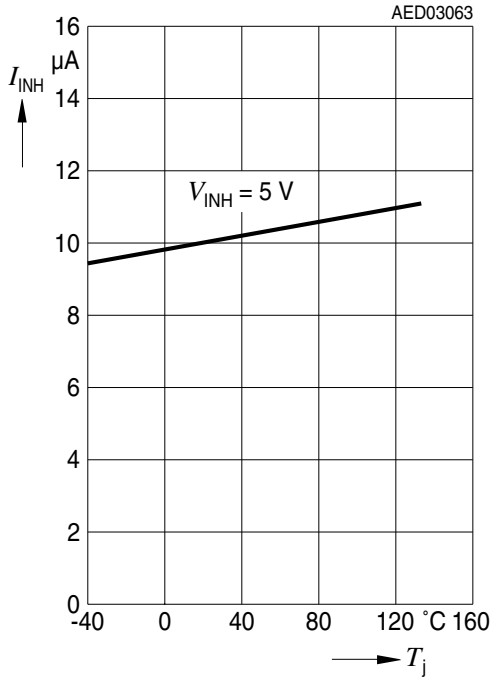
Electrical Characteristics Voltage Regulator

V_I = 13.5 V, -40 °C ≤ T_j ≤150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.5.1	Switching Voltage	$V_{INH,ON}$	3.6	–	–	V	IC turned on
5.5.2	Turn-OFF Voltage	$V_{INH,OFF}$	–	–	0.8	V	IC turned off
5.5.3	Inhibit Input Current	I_{INH}	5	10	27	µA	V_{INH} = 5 V

5.6 Typical Performance Characteristics Inhibit

Inhibit Input Current I_{INH} versus Junction Temperature T_j



5.7 Reset Function

Electrical Characteristics Reset Function

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, V_{INH} > 3.6 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

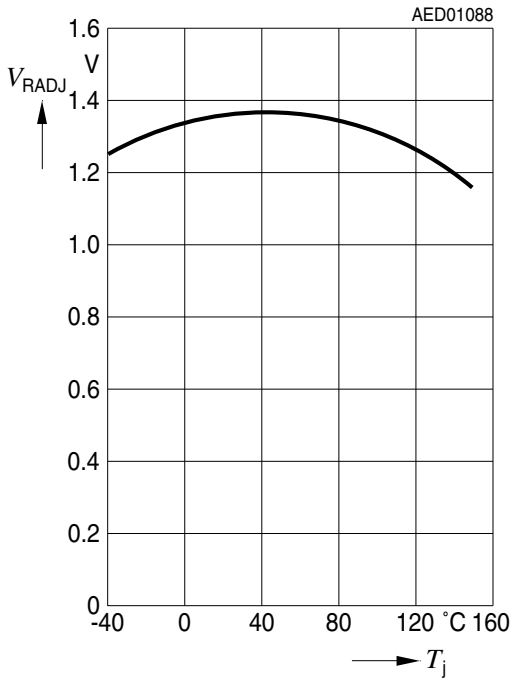
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output Undervoltage Reset							
5.7.1	Default Output Undervoltage Reset Switching Thresholds	$V_{Q,rt}$	4.5	4.65	4.8	V	V_Q decreasing
Output Undervoltage Reset Threshold Adjustment							
5.7.2	Reset Adjust Switching Threshold	$V_{RADJ,th}$	1.26	1.36	1.44	V	3.5 V ≤ V_Q < 5 V
5.7.3	Reset Adjustment Range[1)]	$V_{RT,range}$	3.50	–	4.65	V	–
Reset Output RO							
5.7.4	Reset Output Low Voltage	$V_{RO,low}$	–	0.1	0.4	V	I_{RO} = 1 mA
Reset Delay Timing							
5.7.5	Power On Reset Delay Time	t_{rd}	1.3	2.8	4.1	ms	C_D = 100 nF
5.7.6	Saturation Voltage	$V_{D,sat}$	–	50	110	mV	V_Q < $V_{R,th}$
5.7.7	Upper Delay Switching Threshold	V_{DU}	1.40	1.70	2.20	V	–
5.7.8	Lower Delay Switching Threshold	V_{DRL}	0.20	0.35	0.59	V	–
5.7.9	Delay Capacitor Charge Current	$I_{D,ch}$	40	60	88	µA	–
5.7.10	Reset Reaction Time	t_{rr}	0.5	1.2	4	µs	C_D = 100 nF

1) V_{RT} is scaled linearly, in case the Reset Switching Threshold is modified

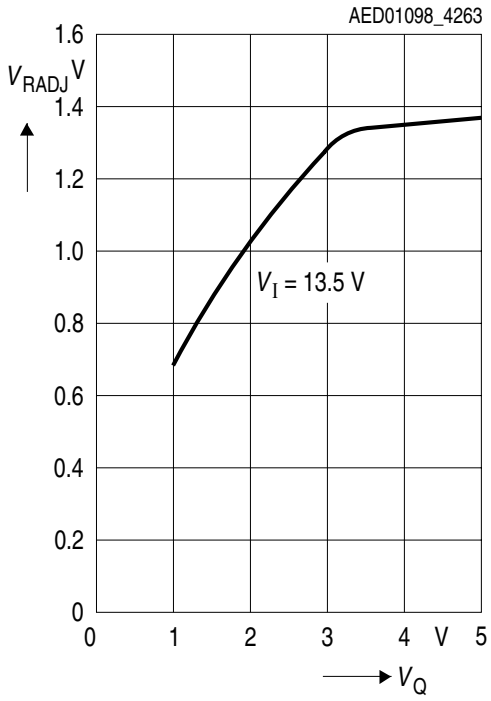
Note: The reset output is low within the range V_Q = 1 V to $V_{Q,rt}$

5.8 Typical Performance Characteristics Reset

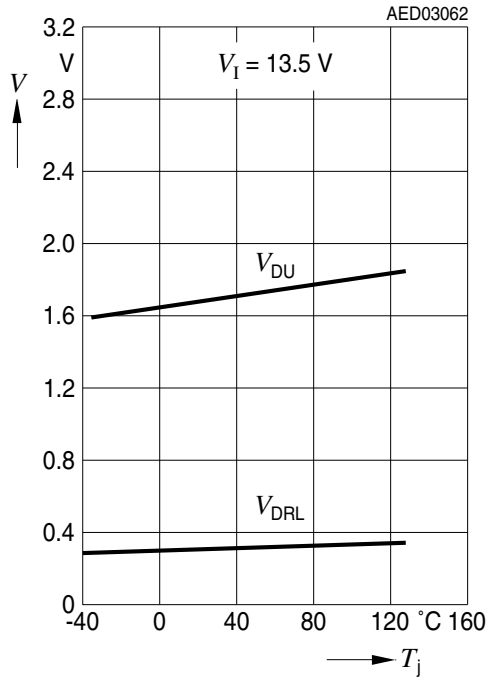
Undervoltage Reset Adjust Threshold V_{RT} versus Junction Temperature T_j



Undervoltage Reset Adjust Threshold $V_{RADJ,th}$ versus Output Voltage V_Q



Timing Threshold Voltage V_{DU} and V_{DRL} versus Temperature



5.9 Watchdog Function

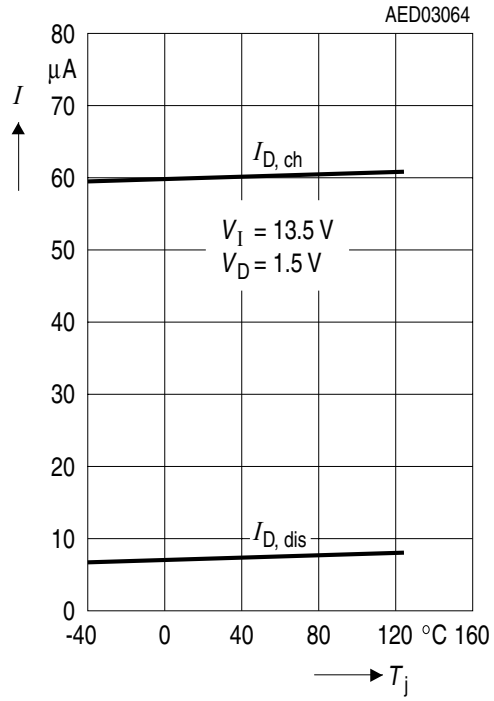
Electrical Characteristics Watchdog Function

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, V_{INH} > 3.6 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

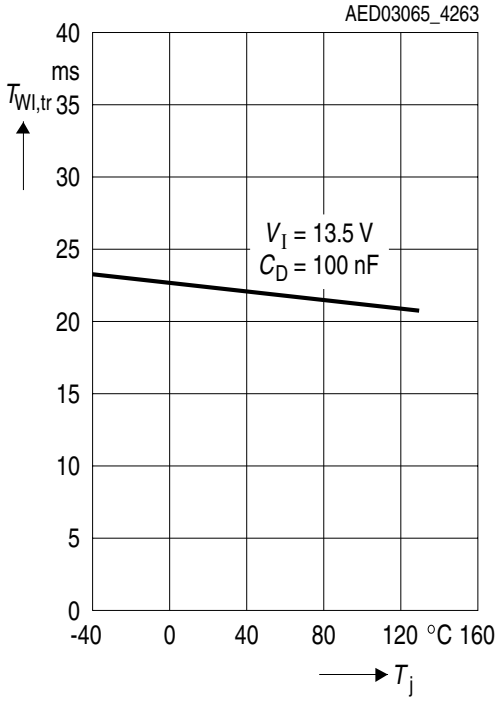
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.9.1	Discharge Current	$I_{D,wd}$	4.40	6.25	9.40	µA	V_D = 1.0 V
5.9.2	Upper Timing Threshold	V_{DU}	1.40	1.70	2.20	V	–
5.9.3	Lower Timing Threshold	V_{DWL}	0.20	0.35	0.55	V	–
5.9.4	Watchdog Trigger Time	$T_{WI,tr}$	16	22.5	27	ms	C_D = 100 nF $V_Q > V_{Q,RT}$
5.9.5	Watchdog Output Low Time	$T_{WD,L}$	1	2.1	3.5	ms	C_D = 100 nF $V_Q > V_{Q,RT}$
5.9.6	Watchdog Period $T_{WI,p} = T_{WD,L} + T_{WI,tr}$	$T_{WI,p}$	17	24.6	30.5	ms	C_D = 100 nF $V_Q > V_{Q,RT}$

5.10 Typical Performance Characteristics Watchdog

Charge Current and Discharge Current versus Temperature



Watchdog Trigger Time versus Temperature



6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

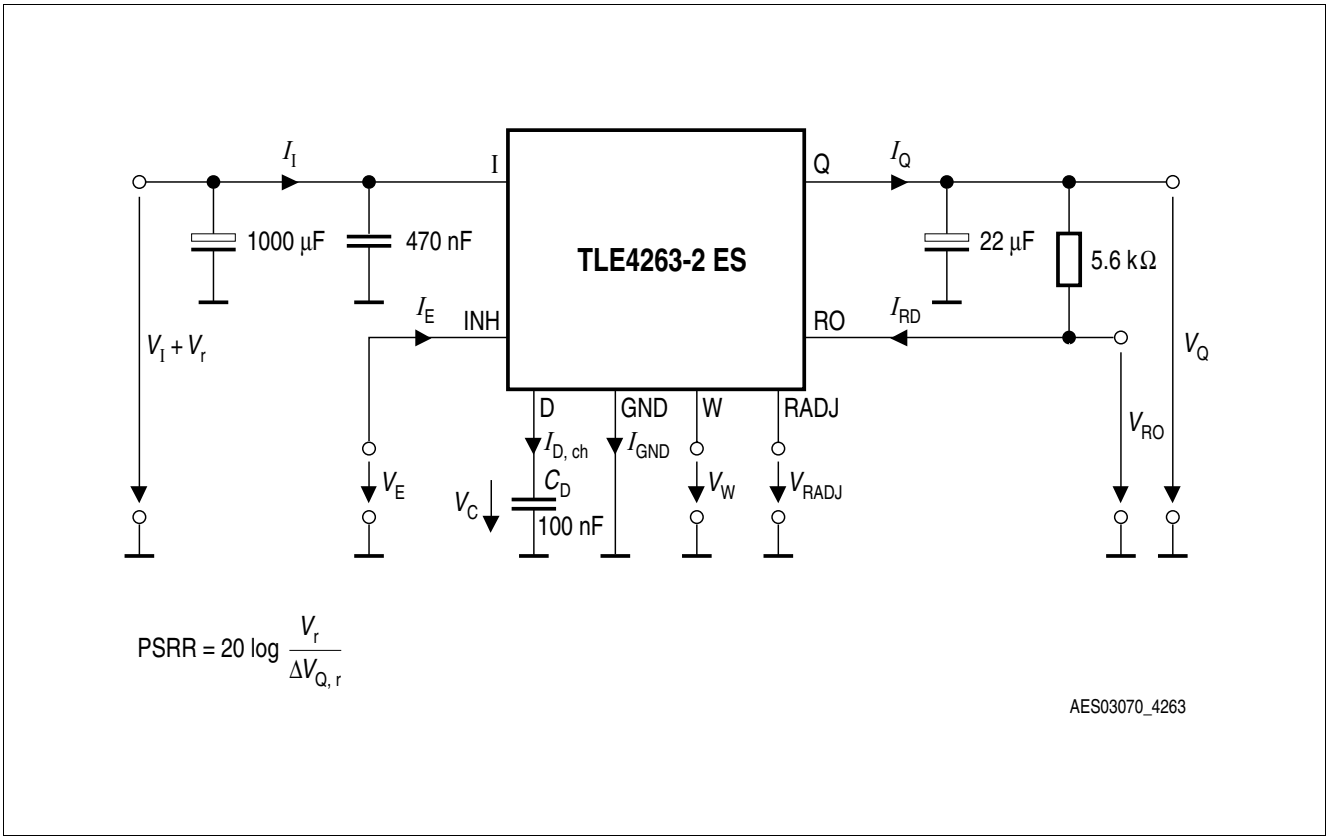


Figure 3 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

6.1 Reset

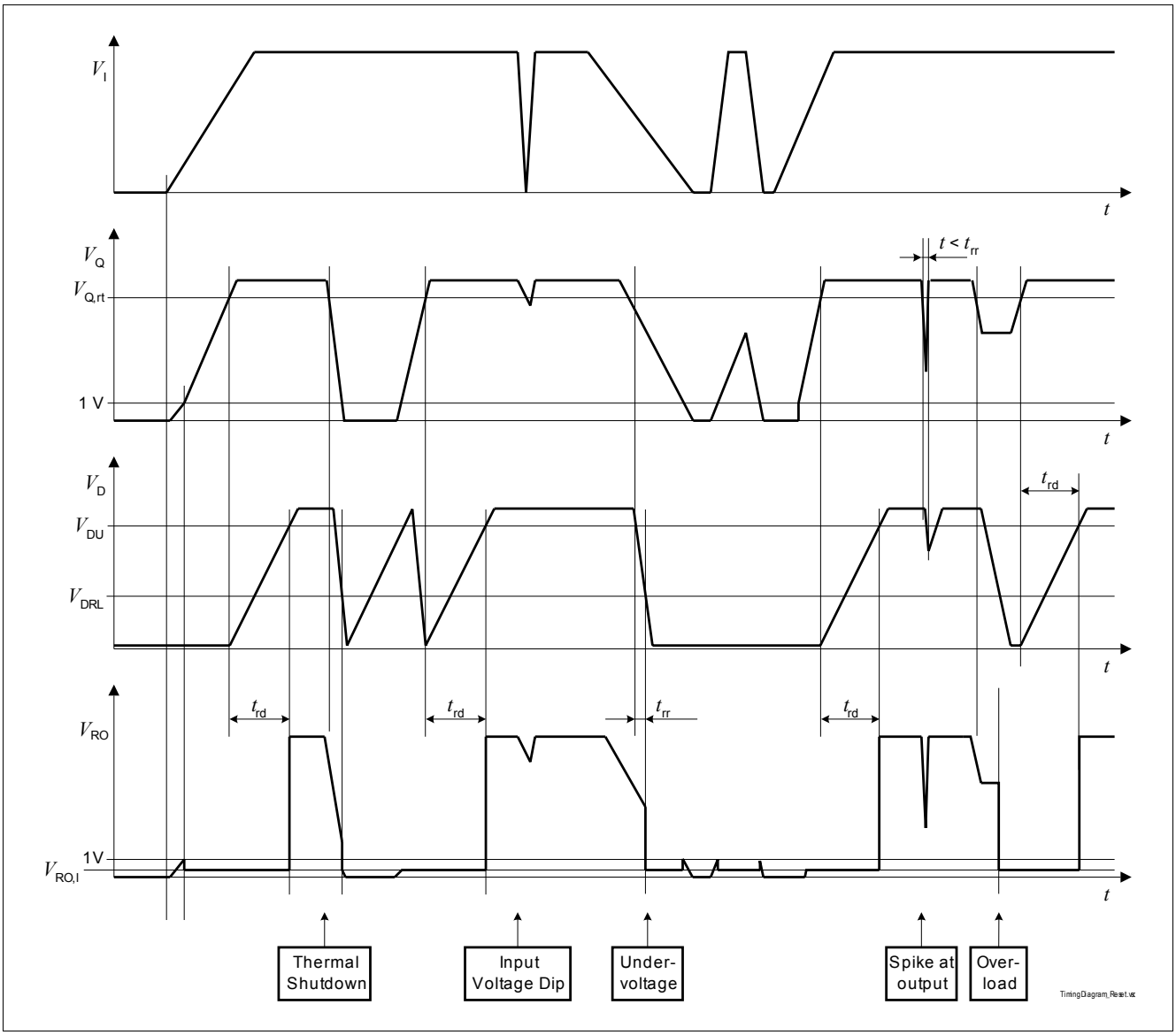


Figure 4 Reset Timing Diagram

Power-On Reset Delay Time

If the application needs a power-on reset delay time t_{rd} different from the value given in **Item 5.7.5**, the delay capacitor's value can be derived from these specified values and the desired power-on delay time:

$$C_D = \frac{t_{rd,\,new}}{t_{rd}} \times 100\,nF$$

with

- C_D: capacitance of the delay capacitor to be chosen
- $t_{rd,new}$: desired power-on reset delay time
- t_{rd}: power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor's tolerance into consideration.

Reset Adjust Function

The undervoltage reset switching threshold can be adjusted according to the application's needs by connecting an external voltage divider (R_{ADJ1}, R_{ADJ2}) at pin RADJ. For selecting the default threshold connect pin RADJ to GND.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,new}$ is calculated as follows:

$$V_{RT,new} = \frac{R_{ADJ,1} + R_{ADJ,2}}{R_{ADJ,2}} \times V_{RADJ,th} \quad (1)$$

with

- $V_{RT,new}$: the desired new reset switching threshold
- R_{ADJ1}, R_{ADJ2}: resistors of the external voltage divider

$V_{RADJ,th}$: reset adjust switching threshold given in **"Reset Function" on Page 13**

6.2 Watchdog

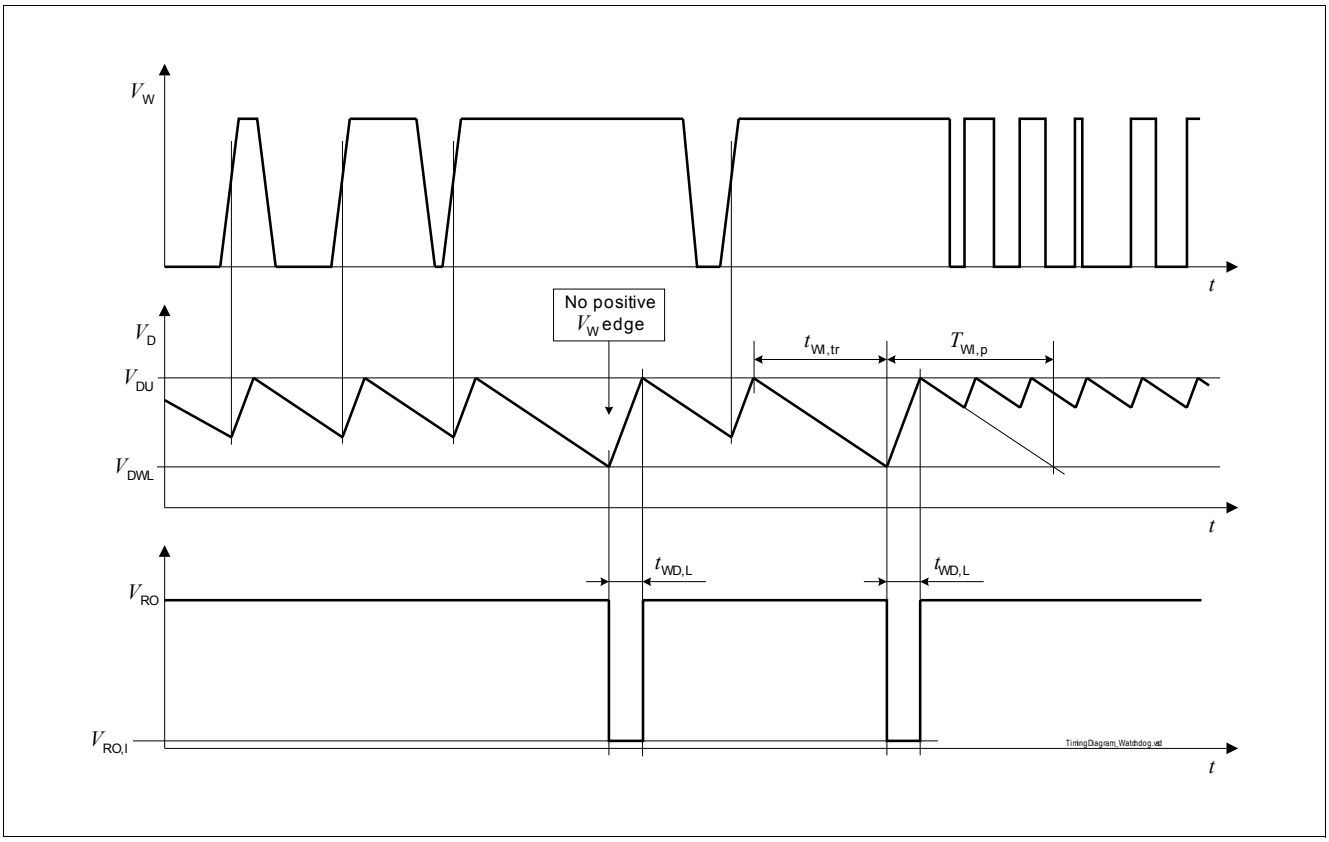


Figure 5 Timing of the Watchdog Function Reset

Watchdog Timing

The period of the watchdog pulses has to be smaller than the minimum watchdog trigger time which is set by the external reset delay capacitor C_D. Use the following formula for dimensioning C_D:

$$C_D = \frac{T_{WI,tr,new}}{T_{WI,tr}} \times 100\ nF \quad (2)$$

with

- C_D: capacitance of the delay capacitor to be chosen
- $T_{WI,tr,new}$: desired watchdog trigger time
- $T_{WI,tr}$: watchdog trigger time specified in this data sheet

7 Package Outlines

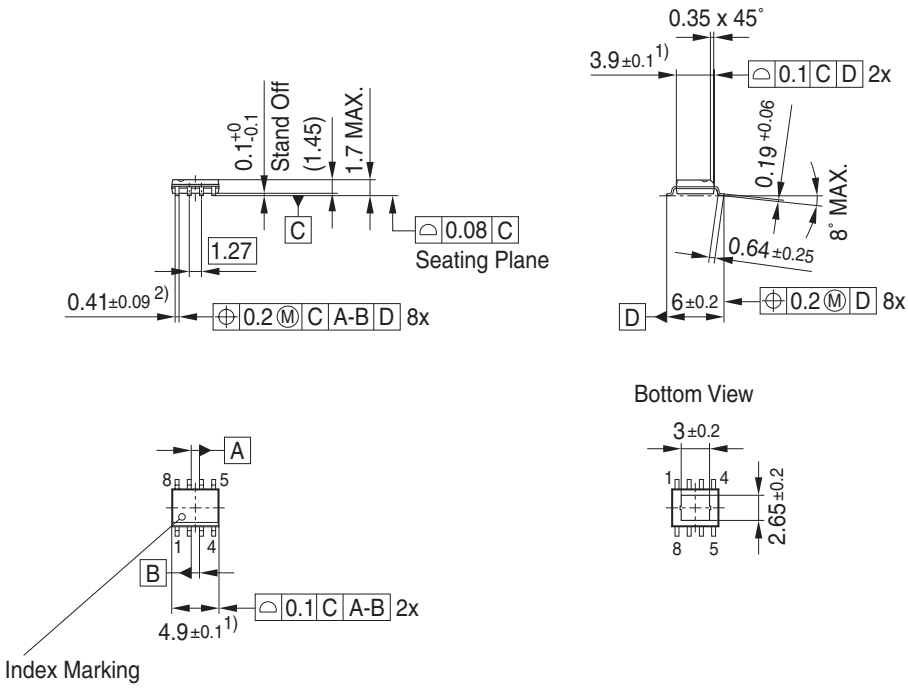


Figure 6 PG-DSO-8 exposed pad

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

8 Revision History

Revision	Date	Changes
1.0	2008-04-21	final version data sheet

Edition 2008-04-21

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Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

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